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CALCULATION OF SEMICONDUCTOR FAILURE RATE

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ABSTRACT: The Performance One of the fundamentals of understanding a product's reliability requires an understanding of the calculation of the failure rate. The traditional method of determining a product's failure rate is through the use of accelerated high temperature operating life tests performed on a sample of devices randomly selected from its parent population. The failure rate obtained on the life test sample is then extrapolated to end-use conditions by means of predetermined statistical models to give an estimate of the failure rate in the field application. Although there are many other stress methods employed by semiconductor manufacturers to fully characterize a product's reliability, the data generated from operating life test sampling is the principal method used by the industry for estimating the failure rate of a semiconductor device in field service. This article focuses on describing the methods used in calculating the failure rate and ends with showing the failure rates determined for some of Intersil's newer integrated circuit process technologies.
Keywords: Failure rate, MPPF, Confidence level, Activation Energy.

I. INTRODUCTION

The requirements concerning quality and reliability of products are always increasing. It is not sufficient to only deliver fault-free parts. In addition, it must be ensured that the delivered goods serve their purpose safely and failure free, i.e., reliably. From the delivery of the device and up to its use in a final product, there are some occasions where the device or the final product may fail despite testing and outgoing inspection. In principle, this sequence is valid for all components of a product. For these reasons, the negative consequences of a failure, which become more serious and expensive the later they occur, are obvious.

The manufacturer is therefore interested in supplying products with the lowest possible

1.1 AVERAGE OUTGOING QUALITY (AOQ)

All outgoing products are sampled after 100 % testing. This is known as "Average Outgoing Quality" (AOQ). The results of this inspection are recorded in ppm (parts per million) using the method defined in JEDEC 16.

1.2 EARLY FAILURE RATE (EFR)

EFR is an estimate (in ppm) of the number of early failures related to the number of devices used. Early failures are normally those which occur within the first 300 to 1000 h.
Essentially, this period of time covers the guarantee period of the finished unit. Low EFR values are therefore very important to the device user. The early life failure rate is heavily influenced by complexity. Consequently, 'designing-in' of better quality during the development and design phase, as well as optimized process control during manufacturing, significantly reduces the EFR value.
Normally, the early failure rate should not be significantly higher than the random failure rate. EFR is given in ppm (parts per million).

1.3 LONG-TERM FAILURE RATE (LFR)

LFR shows the failure rate during the operational period of the devices. This period is of particular interest to the manufacturer of the final product. Based on the LFR value, estimations concerning long-term failure rate, reliability and a device's or module's usage life may be derived. The usage life time is normally the period of constant failure rate. All failures occurring during this period are random Within this period the failure rate is

$$\lambda = \frac{\text{sum of failure}}{\sum(\text{Quantity} \times \text{Time to failure})} \times \frac{1}{\text{h}} \quad (1)$$

The measure of λ is FIT (Failures in Time = number of failures in 10^9 device hours).

EXAMPLE
A sample of 500 semiconductor devices is tested in a operating life test (dynamic electric operation). The devices operate for a period of 10 000 h.
Failures: 1 failure after 1000 h
1 failure after 2000 h
The failure rate may be calculated from this sample by

$$\lambda = \frac{2}{1\times1000 + 1\times2000 + 489\times10000} \times \frac{1}{\text{h}}$$

$$\lambda = \frac{2}{4983000} \times \frac{1}{\text{h}} = 4.01 \times 10^{-7} \frac{1}{h}$$

This is a λ-value of 400 FIT, or this sample has a failure rate of 0.04 %/1000 h on average.

II. CONFIDENCE LEVEL

The failure rate λ calculated from the sample is an estimate of the unknown failure rate of the lot. The interval of the failure rate (confidence interval) may be calculated, depending on the confidence level and sample size.
The following is valid:

The larger the sample size, the narrower the confidence interval. The lower the confidence level of the statement, the narrower the confidence interval.

The confidence level applicable to the failure rate of the whole lot when using the estimated value of λ is derived from the x^2-distribution. In practice, only the upper limit of the confidence interval (the maximum average failure rate) is used.

$$\lambda_{max} = \frac{x^2/2(r, P_A)}{n \times t} \text{in } \frac{1}{\text{h}} \quad (2)$$

$$\text{LFR} = \frac{x^2/2(r, P_A)}{n \times t} \times 1 \times 10^9 \text{ in[FIT]} \quad (3)$$

r: Number of failures
P_A: Confidence level
n: Sample size
t: Time in hours
n x t: Device hours
The $\chi^2/2$ for λ are taken from table 1. For the above example from table 1
$\chi^2/2$ (r = 2; PA = 60 %) = 3.08
n x t = 4983000 h

$$\lambda_{max} = \frac{3.08}{4983000} = 6.18 \times 10^{-7} \frac{1}{\text{h}}$$

This means that the failure rate of the lot does not exceed 0.0618 %/1000 h (618 FIT) with a probability of 60 %. If a confidence level of 90 % is chosen from the table 1 :
χ2/2 (r = 2; PA = 90 %) = 5.3

$$\lambda_{max} = \frac{5.3}{4983000} = 1.06 \times 10^{-6} \frac{1}{\text{h}}$$

This means that the failure rate of the lot does not exceed 0.106 %/1000 h (1060 FIT) with a probability of 90 %.

Table 2. 1. No. of failures v/s Confidence level

NUMBER OF FAILURE	CONFIDENCE LEVEL			
	50	60	90	95
0	0.60	0.93	2.31	2.96
1	1.68	2.00	3.89	4.67
2	2.67	3.08	5.30	6.21
3	3.67	4.17	6.70	7.69
4	4.67	5.24	8.00	9.09
5	5.67	6.25	9.25	10.42
6	6.67	7.27	10.55	11.76
7	7.67	8.33	11.75	13.16
8	8.67	9.35	13.00	14.30
9	9.67	10.42	14.20	15.63
10	10.67	11.42	15.40	16.95

III. OPERATING LIFE TESTS

Number of devices tested: n = 50
Number of failures
(positive qualification): c = 0
Test time: t = 2000 h
Confidence level: PA = 60 %
$x^2/2$ (0; 60 %) = 0.93

$$\lambda_{max} = \frac{0.93}{50 \times 2000} = 9.3 \times 10^{-6} \frac{1}{\text{h}}$$

This means, that the failure rate of the lot does not exceed 0.93 %/1000 h (9300 FIT) with a probability of 60 %. This example demonstrates that it is only possible to verify LFR values of 9300 FIT with a confidence level of 60 % in a normal qualification tests (50 devices, 2000 h). To obtain LFR values which meet today's requirements (< 50 FIT), the following conditions have to be fulfilled:
Very long test periods
Large quantities of devices
Accelerated testing (e.g., higher temperature)

IV. MEAN TIME TO FAILURE (MTTF)

For systems which cannot be repaired and whose devices must be changed, e.g., semiconductors, the following is valid:

$$\text{MTTF} = \frac{1}{\text{h}} \quad (4)$$

V. ACCELERATING STREES TEST

Innovation cycles in the field of semiconductors are becoming shorter and shorter. This means that products must be brought to the market quicker. At the same time, expectations concerning the quality and reliability of the products have become higher. Manufacturers of semiconductors must therefore assure long operating periods with high reliability but in a short time. Sample stress testing is the most commonly used way of assuring this.

$$\lambda \infty \frac{1}{\text{TDH} \times \text{AF}} \quad (5)$$

Where
λ = failure rate.
TDH = Total Device Hours = Number of units x hours under stress.
AF = Acceleration factor

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanisms in a life test, since the failure mechanisms are thermally activated at different rates. Equation 1 accounts for these conditions and includes a statistical factor to obtain the confidence level for the resulting failure rate.

$$\lambda = \sum_{i-1}^{\beta} \left(\frac{x_i}{(\sum_{j=1}^{k} \text{TDH}_j \times \text{AF}_{ij})} \right) \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i} \quad (6)$$

Where,
λ = failure rate in FITs (Number fails in 10^9 device hours)
β = Number of distinct possible failure mechanisms
k = Number of life tests being combined
x_I = Number of failures for a given failure mechanism
i = 1, 2,... β

TDH_j = Total device hours of test time for life test j,
j = 1, 2...k
AF_{ij} = Acceleration factor for appropriate failure mechanism, i = 1, 2... k
M= $\chi^2/2$ (r; PA), the $\chi^2/2$ for λ are taken from table 1.

In the failure rate calculation, acceleration factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. The acceleration factor is determined from the Arrhenius equation. This equation is used to describe physio-chemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor device failure mechanisms.

$$AF = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right) \quad (7)$$

Where,
AF = Acceleration Factor
Ea = Thermal Activation Energy (Table 2)
k = Boltzmann's Constant (8.63 x 10 -5 eV/K)
T_{use} = Use Temperature (°C + 273)
T_{stress} = Life test stress temperature (°C + 273)
Both T_{use} and T_{stress} (in degrees Kelvin) need to include the internal temperature rise of the device to represent the junction temperature of the chip under bias.

VI. ACTIVATION ENERGY

There are some conditions which need to be fulfilled in order to use Arrhenius method:

The validity of Arrhenius rule has to be verified.
Failure-specific activation energies must be determined.
These conditions may be verified by a series of tests. Today, this procedure is generally accepted and used as a basis for estimating operating life. The values of activation energies can be determined by experiments for different failure mechanisms.
Values often used for different device groups are:

Bipolar ICs 0.7 eV
MOS ICs 0.6 eV
Transistors 0.7 eV
Diodes 0.7 eV

By using this method, it is possible to provide long-term predictions for the actual operation of semiconductors even with relatively short test periods.

VII. CONCLUSION

The above is a simple introduction to general ideas about reliability, reliability tests, and derating and forecasting of reliability of high power semiconductor, which are semiconductor devices for electric power. As explained above, it is vital for higher reliability in practical use of semiconductor devices to understand their features and select those which are suitable for equipment and sets. Also important to design semiconductor devices with some allowance to improve reliability, fully taking their derating into consideration in relation to operating and environmental conditions. Other essential thing to do is to "debug" equipment and sets, and to analyze data obtained in fabrication process and actual operation to feed them back to design and fabrication stages. To improve the reliability by design of high power semiconductor requires considerations on many issues as described above. Utilize the semiconductor devices successfully with the utmost care with comprehensive understanding of their quality, reliability, and economy.

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