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ASSESSMENT OF ANALOG PERFORMANCE OF AN ASYMMETRIC GATE STACK D. G. MOSHEMT WITH RESPECT TO SOURCE END UNDERLAP LENGTH

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Abstract: ***This paper presents a systematic comparative study of analog performances of an under lapped double gate (U-DG) MOSHEMT's with Gate Stack (GS) with varying underlap length. In highly scaled devices, conventionally, symmetric underlap is used at the Source and Drain side so as to reduce the short channel effects (SCE's). However, this leads to increased channel resistance decreasing the ON current. Asymmetric underlap devices (A -U-DG) have been proposed as one of the remedies with underlap being present only at the source side. Different parameters such as drain characteristics, transfer characteristics, transconductance (gm), transconductance generating factor (gm/Id) and output resistance (Ro) have been analyzed for various underlap lengths. For optimization of the desired underlap length, the DIBL and the Ion / Ioff ratio have been considered. Analysis suggested that the device with underlap length of 24 nm shows superior Analog Performance in terms of better Ion / Ioff ratio and better resistance to SCE's. Thus, the optimal underlap length is 24 nm.***

Keywords: Gate stack; asymmetric underlap; analog performance; DG MOSHEMT's

I. INTRODUCTION

RECENTLY, AlInN/GaNhetrostructure has emerged as a superior alternative to the conventional AlGaN/GaNhetrostructure based High Electron Mobility Transistors (HEMTs) and metal oxide semiconductor HEMTs (MOS-HEMTs) [1-4]. The lattice matched in AlInN/GaN structure offers much better performance than the AlGaN/GaN structure. The devices deploying AlInN/GaN have higher spontaneous polarization induced two-dimensional electron gas (2DEG) density [5], higher drain current (ID) and the structure is stress-free with enhanced reliability, and better thermal and chemical stability [3]. AlxIn1−xN with Al composition of about 0.83 is nearly lattice-matched to GaN and superior-quality AlInN/GaNhetrostructure have been grown by metal-organic vapor phase epitaxy (MOVPE) [7]. Devices using AlInN/GaN have shown very high electron mobility (1200 to 2000 cm2/Vs) and high 2DEG sheet carrier densities (3.2x1013cm−2) [7-8].Considering the enormous potential of AlInN/GaNhetrostructure it has deployed in the present work. The Double gate (DG) MOSFET with asymmetric source underlap at the source side suffers from SCE's owing to high scaling [6-7]. Symmetric underlap is introduced to reduce SCE's like Drain Induced Barrier Lowering (DIBL) [8-9]. Gate Induced Drain Leakage (GIDL) and fringing of underlap [10]. However, owing to increased effective channel length, the channel resistance increases and as a result, the on current (Ion) gets affected. But the foremost demand from a device used in System on Chip (SoC) applications is a high value of Ion [11]. So to reduce channel resistance, Asymmetric Underlap Double Gate MOSHEMT with Gate Stack (A-U-DG- MOSHEMT) is proposed as a modification to the conventional U-DG-MOSHEMT. Here, the underlap is only present at the source side. This reduces the channel resistance and correspondingly improves Ion. The main objective of the paper is to provide a comparative study between Asymmetric Underlap Double Gate MOSHEMT with Gate Stack (A-U-DG-GS MOSHEMT) devices with different underlap lengths. Different parameters such as the drain current (ID), transconductance (gm), the transconductance generation factor (gm/ID) and the output resistance (ro) are analyzed to judge the device performances. The optimization of the desired underlap length is assessed on the basis of the FOM: Ion / Ioff ratio.

The thickness of oxide layer has a major influence on the performance of MOS-HEMTs. The effect of high-k oxides such as Al2O3, ZrO2 and HfO2on the gate current leakage of MOS-HEMT devices are analyzed by few group [3-4]. Other than that no major has been done in this area. Considering the utility of underlap DG MOS-HEMT devices for high speed and high power application, the comprehensive investigation analyzing the effect oxide thickness on performance of AlInN A-U-DG- MOSHEMT is of paramount significance. Thus, in this paper for the first time, we analyze the effect of Al2O3 thickness on the performance of the AlInN/GaN A-U-DG- MOSHEMT. Extensive device simulations of transfer characteristics, output characteristics, transconductance (gm), transconductance generation factor (TGF).

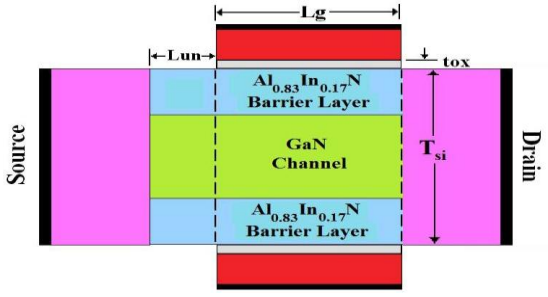

Fig1. Cross sectional view of AlInN/GaNHetrostructure Gate Stack A-U-DG- MOSHEMT The channel consists of undoped narrow bandgapGaN (TC=10nm) region and two wide bandgap barrier Al0.83In0.17N (TB=3 nm) regions. Source/drain region doping is 1020cm3 with 5nm length. The gate length Lg=18nm and Al2O3 gate dielectric is constant. source end Lun varied from 18 nm to 24 nm in steps of 3nm.
The highly scaled devices also suffer from SCE's owing to high scaling [17-18]. Asymmetric source underlap is introduced to reduce SCE's like Drain Induced Barrier Lowering (DIBL) [19-20]. Gate Induced Drain Leakage (GIDL) and fringing capacitance are also reduced with the introduction of underlap [21]. However, owing to increased effective channel length, the channel resistance increases and as a result, the on current (Ion) gets affected. But the foremost demand from a device used in System on Chip (SoC) applications is a high value of Ion [22]. So to reduce channel resistance, Asymmetric Underlap Double Gate MOSHEMT with Gate Stack (A-U-DG-GS MOSHEMT) is proposed as a modification to the conventional U-DG-MOSHEMT. Here, the underlap is only present at the source side. This reduces the channel resistance and correspondingly improves Ion. The main objective of the paper is to provide a comparative study between Asymmetric Underlap Double Gate MOSHEMT with Gate Stack (A-U-DG-GS NMOSFET) devices with different underlap lengths. Different parameters such as the drain current (ID), transconductance (gm), the transconductance generation factor (gm/ID) and the output resistance (ro) are analyzed to judge the device performances. The optimization of the desired underlap length is assessed on the basis of the FOM: DIBL and Ion / Ioff ratio.

II. DEVICE DESCRIPTION AND SIMULATION

All the device parameters and supply voltage used for the device simulations are in accordance with the ITRS Roadmap for RF and Mixed Signal Applications [23]. All simulations have been performed using Sylvaco TCAD, a 2-D device simulator, using the standard density gradient model [24]. The device structure under consideration is shown in Fig. 1. An asymmetric underlap double gate MOSHEMT. with Gate Stack (A-U-DG-GS) is taken as the base device for simulation where the channel doping concentration is fixed at 1015 cm-3 and a doping concentration of 1020 cm-3 is chosen for the source and drain region. The device has a gate length (Lg) of 18 nm. The underlap is present only on the Source side (Lun). For optimization, the underlap lengths of 18 nm, 21 nm and 24 nm have been considered. The silicon body thickness (tsi) is about 16 nm whereas the gate height is 9.1 nm. The EOT of the device is 0.9 nm [14], which is achieved by using an interfacial layer (Tox_low) of SiO2 of 0.45 nm and an oxide layer (Tox_high) of HfO2 of about 2.9 nm. The HfO2 layer is placed over the SiO2 layer which provides higher physical gate height to the device. The foundation device is a nitride spacer.

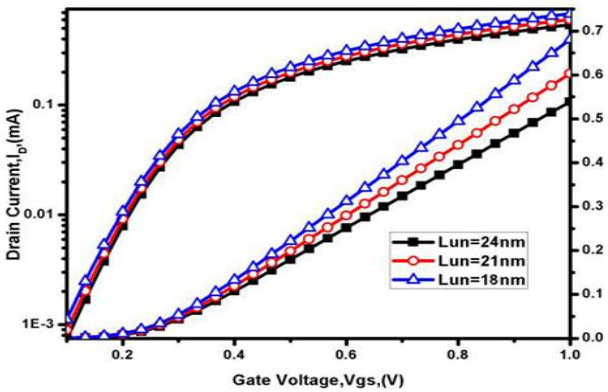

Fig. 2. Comparison of Id of A-U-DG-GS MOSHEMT with various underlap lengths as a function of Vgs, at Vds = 0.5 V the device with 21 nm underlap shows lower on current and the device with 24 nm underlap shows the least on current.

III. RESULTS AND DISCUSSIONS

The Analog performance of the A-U-DG-GS NMOSFET is analyzed in this section. The underlap lengths have been varied from 18 nm to 24 nm. The analog parameters analyzed here are Ids, gm, gm/Ids, ro and gm,ro. The transfer characteristics curves of the three devices are analyzed from Fig. 2. It is observed that the device with an underlap of 18 nm shows a greater on current for a given value of gate voltage. The device with 21 nm underlap shows a lesser on current and the device with 24 nm underlap shows the least on current for a given gate voltage.

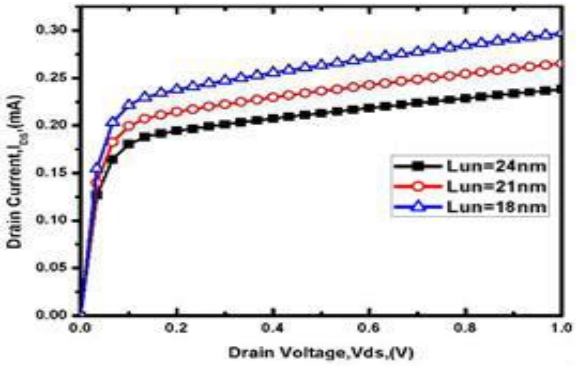

Fig. 3: Comparison of Id of A-U-DG-GS MOSFET with various underlap lengths as a function of Vgs, at Vds = 0.5 V.

The barrier height of the device with 24 nm underlap is greater than the barrier height of the device with 21 nm underlap, and the device with 18 nm underlap shows the least barrier height. Greater barrier heights suggest lower on currents. Thus, the device with 18 nm underlap shows the highest on current, The Ids-Vds curves of the three devices are presented. It is inferred from the figure that lower the underlap length, higher is the drain current,

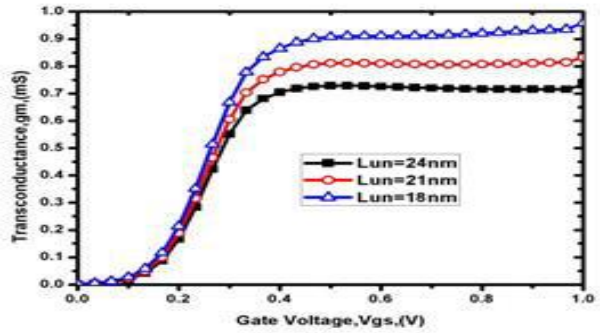

Fig. 4. Comparison of gm of A-U-DG-GS MOSHEMT with various underlap lengths as a function of Vgs, at Vds = 0.5 V.

The parameter gm, depends upon Vgs and Id, at a fixed Vds. Since the gate biasing Vgs is same for all the devices it is the Id which is responsible for the variation in gm in the devices. Thus, the device with higher Id also has a higher gm. The variation of Conduction Band Energy for various underlap lengths of the A-U-DG-GS MOSHEMT device as a function of distance along

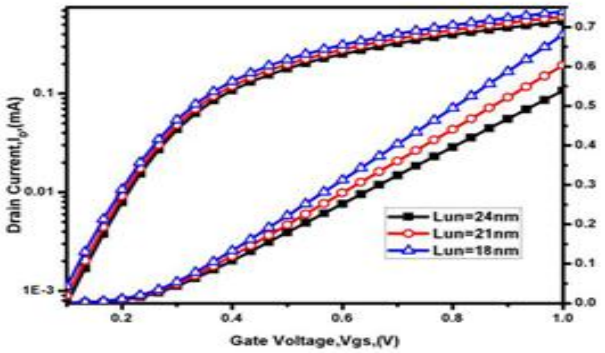

Fig. 5 compares the gm/Id curves of the three devices. Since the device with 18 nm underlap shows both the highest drain current and the highest gm, it shows the least gm/Id. Similarly, the device with 21 nm underlap shows slightly higher gm/Id and the device with 24 nm underlap shows the maximum gm/Id.

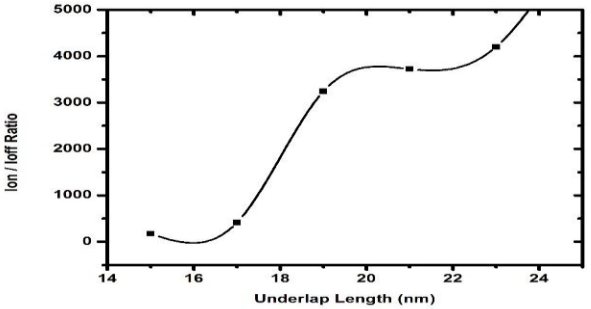

Fig. 6. Variation of Ion/Ioff ratio of A-U-DG-GS MOSHEMT for various underlap lengths.

Fig. 6 shows the variation of the Ion/Ioff ratio of the devices with respect to their underlap lengths. The device with an underlap length of 24 nm displays the highest Ion/Ioff ratio while the device with the 18 nm underlap displays the lowest Ion/Ioff ratio. Variation of Ion/Ioff ratio of A-U-DG-GS MOSHEMT for various underlap lengths, which is consistent with the theory that a greater effective channel length increases the channel resistance, thus reducing the ION.

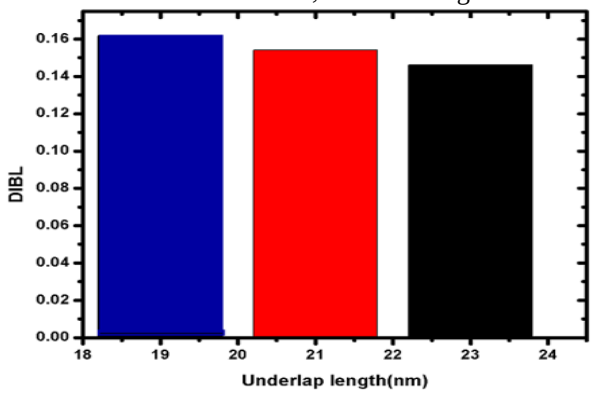

Fig. 7. DIBL for various underlap lengths of A-U-DG-GS MOSHEMT atVds = 0.5 V and Vgs = 1 V.

Fig. 7 lists the DIBL values of the three devices. The device with 24 nm underlap displays the least DIBL while the device with 18 nm underlap shows the maximum DIBL. This is because the underlap provides a screening effect from the drain bias and thus prevents the barrier lowering caused by the drain bias.

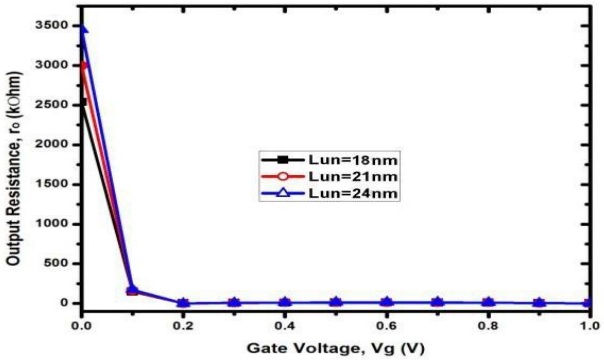

Fig. 8 compares the output resistance of the three devices. Greater the underlap, greater is the output resistance. Thus, the device with 18 nm underlap shows minimum ro, the device

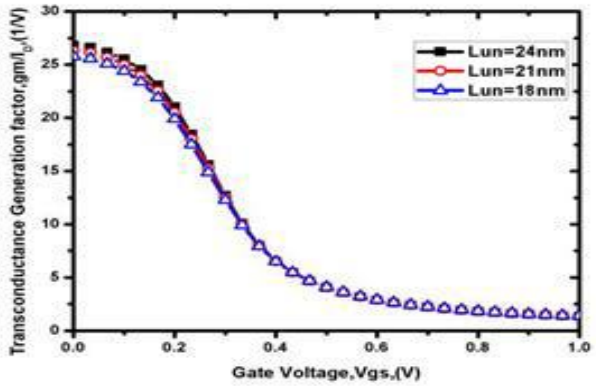

Fig. 9.Comparison of ro of A-U-DG-GS MOSHEMT with various underlap lengths as a function of Vgs at Vds = 0.5 V.

IV. CONCLUSION

In this work, the optimization of underlap length in an A-U-DG-GS MOSHEMT is presented. On comparing the characteristics of the three devices, it is observed that the Ion is increased by reducing the channel length. However, the Ion/Ioff ratio the device with an underlap of 24 nm shows an improvement of 30.78% compared to the device with 18 nm underlap and 14.1% compared to the device with an underlap of 21 nm. Furthermore, scaling down the device greatly increases the risk of Short Channel Effects. The device with 18nm underlap is most susceptible to SCE's. The device with an underlap of 24 nm shows a 9.6% lesser DIBL than the device with an underlap of 18 nm and 4.2% lesser DIBL than the device with an underlap of 21 nm. Considering all these factors, the use of 18 nm underlap in an A-U-DG-GS MOSHEMT is discouraged. The underlap of 24 nm offers superior performance on all parameters is hence preferred.

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