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SURVEY ON LOW-LATENCY AND LOW-POWER SCHEMES FOR ON-CHIP NETWORKS

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Abstract: Network on-chip (NoC) has emerged as a vital factor that determines the performance and power consumption of many-core systems. This paper presents a survey on different low-latency & low-power NoC architectures and techniques, such as the routing algorithms, buffer less router architecture, source synchronous bypass architecture, switching techniques, butterfly and regular reconfigurable topologies, constraints mapping onto NoC and the protocols used for allocating routes in an on-chip network. Then finally, a hybrid scheme for NoC, which uses switching mechanism, called virtual circuit switching, is proposed to intermingle with circuit switching and packet switching. A path allocation algorithm is proposed to determine VCS connections and circuit-switched connections on a mesh-connected NoC, such that both communication latency and power are optimized.

Index Terms: Hybrid scheme, low latency, low power, network-on-chip (NoC), virtual circuit-switched (VCS) connections.

I. INTRODUCTION

With the rapid development of advanced nanometer IC technology, continuously shrinking transistor dimensions allow designers to integrate an increasing number of processors or IP cores into a single chip. Traditional bus-based communication is no longer suitable due to its poor scalability. Instead, network-on-chip (NoC) has emerged as a scalable and promising solution to global communications within large multicore systems. Packet-switched (PS) NoCs bring the advantage of high flexibility and high bandwidth to communications [1]. However, such merit is achieved by exploiting a complex router pipeline. The pipeline stages of a baseline PS router include the buffer write (BW) stage, the route computation (RC) stage, the virtual channel allocation (VA) stage, the switch allocation (SA) stage, and the switch traversal (ST) stage. On the one hand, the complex router pipeline leads to a high latency ratio. Although lookahead routing and aggressive speculation shorten the critical path through the router stages, the PS router still occupies a high ratio of communication latency when compared with one-cycle link delay in a mesh-connected NoC. On the other hand, the complex router pipeline leads to a high power ratio.
In comparison with PS NoC, circuit switching [2] can significantly lower the communication latency and power consumption, because routing and arbitration are not needed once circuits are set up. Only the ST stage is required on the circuit-switched (CS) connection when a flit traverses a node. However, circuit switching lacks flexibility. If several communications compete for a common physical channel, circuits will be set up in turn. Then, the long setup time will decrease the overall NoC performance. Further reduction of communication latency and power consumption of NoCs is necessary, because the communication latency of NoCs directly influences the data access latency in many-core systems, and the power consumption of NoCs accounts for a high ratio of the total power consumption of the whole chip. Here, we will propose a novel hybrid scheme, in which a novel switching mechanism, called virtual circuit switching, is first introduced to intermingle with circuit switching and packet switching. In virtual circuit switching, virtual channels (VCs) are exploited to form a number of virtual CS (VCS) connections by storing the interconnect information in routers. Flits can directly traverse the router with only the ST stage. The main advantage of virtual circuit switching is that it can have the similar router pipeline with circuit switching, and can have multiple VCS connections to share a common physical channel. To support the proposed hybrid scheme, one modified router architecture will be implemented based on the baseline with a tolerable overhead, and the corresponding switching mechanism is presented. Based on virtual circuit switching, a path allocation algorithm is proposed to determine VCS connections and CS connections on a mesh-connected NoC under a given network traffic, so that both communication latency and power consumption are optimized [3]. The organization of the rest of the paper is as follows: Section II gives a comparative analysis of different switching schemes & protocols, Section III gives the principle of proposed work, and the conclusion of the paper is given in Section IV.

II. COMPARATIVE ANALYSIS OF DIFFERENT SWITCHING SCHEMES & PROTOCOLS

A. Circuit-switched Coherence

A hybrid router design which intermingles packet-switched flits with circuit-switched flits is proposed since circuit-switched networks can significantly lower the communication latency between processor cores, when compared to packet-switched networks, since once circuits are set up, communication latency approaches pure interconnect delay. However, if circuits are not frequently reused, the long set up time and poorer interconnect utilization can hurt overall performance. Additionally, a co-design prediction-based coherence protocol that leverages the existence of circuits to optimize pair-wise sharing between cores is used. The protocol allows pair wise sharers to communicate directly with each other via circuits and drives up circuit reuse. The hybrid circuit-switched network

used here, successfully overcomes some of the drawbacks associated with circuit switching, specifically, avoiding setup overhead and reconfiguring circuits on-the-fly. And the coherence protocol modifications further drive up circuit reuse and reap higher savings. It has high power overhead due to addition of buffers, switch allocators. The protocol can be evaluated on server consolidation workloads as well as provide more in-depth analysis of the network [4].

B. Processor Allocation mechanism:
A processor allocation mechanism is proposed for run-time assignment of a set of communicating tasks of input applications onto the processing nodes of a Chip Multiprocessor (CMP), when the arrival order and execution lifetime of the input applications are not known a priori. The existing techniques of processor allocation in traditional parallel machines are generally divided into two groups: contiguous and non-contiguous. This takes benefit from the advantages of non-contiguous processor allocation mechanisms, by allowing the tasks of the input application mapped onto disjoint regions (sub-meshes) and then virtually connecting them by bypassing the router pipeline stages of the inter-region routers. The routers in this design are baseline wormhole-switched routers which are slightly modified in order to support VIP connections. VIPs can be considered a kind of circuit-switching scheme. However, they do not suffer from resource utilization and performance degradation (due to the circuit setup time) issues of the conventional circuit-switching. They can be added to a packet-switched NoC in order to improve its performance. Focusing on on-chip communication, this approach used a hybrid switched NoC in which packet-switching and virtual point-to point connections are integrated into the same NoC. The tasks of a single application are mapped onto a virtual region which may consist of several non-contiguous groups of processors. The virtual point-to-point links guarantee low-latency and low-power communication among different parts of a virtual region, while packet switching part handles the traffic inside each contiguous region. In order to achieve better mappings, task migration can be integrated into the algorithm [5].

C. Flattened Butterfly Topology:
With the trend towards increasing number of cores in chip multiprocessors, the on-chip interconnect that connects the cores needs to scale efficiently. The use of high-radix networks in on-chip interconnection networks is proposed and described how the flattened butterfly topology can be mapped to on-chip networks. By reducing the number of routers and channels in the network, it results in a more efficient network with lower latency and lower energy consumption. In addition, it describes the utilization of bypass channels to utilize non-minimal routing with minimal increase in power while further reducing latency in the on-chip network. The flattened butterfly topology is a cost-efficient topology for use with high-radix routers. The flattened butterfly is derived by combining (or flattening) the routers in each row of a conventional butterfly topology while preserving the inter-router connections. The flattened butterfly is similar to a generalized hypercube; however, by providing concentration in the routers, the flattened butterfly significantly reduces the wiring complexity of the topology, allowing it to scale more efficiently [6].

D. Energy & Performance aware-mapping onto NoC:
An algorithm which automatically maps a given set of intellectual property onto a generic regular network-on-chip (NoC) architecture and constructs a deadlock-free deterministic routing function is proposed such that the total communication energy is minimized. At the same time, the performance of the resulting communication system is guaranteed to satisfy the specified design constraints through bandwidth reservation. First formulate the problem of energy- and performance-aware mapping in a topological sense, and show how the routing flexibility can be exploited to expand the solution space and improve the solution quality. An efficient branch-and-bound algorithm is then proposed to solve this problem. Here addressing of the mapping and routing path allocation problems for regular tile-based NoC architectures. An efficient algorithm was proposed, which automatically maps the IPs to tiles and generates a suitable deadlock-free routing function such that the total communication energy consumption is minimized under specified performance constraints. The presented mapping algorithm takes APCG graph as the input, which assumes that the tasks and communication transactions have already been scheduled onto a set of selected IPs. The separation of the scheduling procedure and the mapping routing procedure may lead to the sub-optimality of the solution [7].

E. Bandwidth-Constrained Mapping of Cores onto NoC:
NMAP, a fast algorithm is proposed that maps the cores onto a mesh NoC architecture under bandwidth constraints, minimizing the average communication delay. The NMAP algorithm is presented for both single minimum-path routing and split-traffic routing. The design of complex monolithic systems is addressed, where processing cores generate and consume a varying and large amount of data, thus bringing the communication links to the edge of congestion. Typical applications are in the area of multi-media processing. They considered a mesh-based NoC architecture, and explored the assignment of cores to mesh cross-points so that the traffic on links satisfies bandwidth constraints. A single-path deterministic routing between the cores places high bandwidth demands on the links. The bandwidth requirements can be significantly reduced by splitting the traffic between the cores across multiple paths. The average packet latency with single path and split traffic routing with varying link bandwidths is obtained. As the traffic is bursty in nature, it has contention even when bandwidth constraints are satisfied. The average latency is higher and also increases more sharply with decrease in bandwidth for single path routing. This is because, in single minimum-path routing the congestion on links is higher when compared to the case where the traffic is split across many paths. Moreover, use of wormhole flow control results in a non-linear increase in latency (due to blocking of paths in case of contention,

creating a domino-effect) with decreasing link bandwidth [8].

F. Unified Scheduling and Mapping for General NoCs:
A unified task scheduling and core mapping algorithm called UNISM is proposed for different NOC architectures including regular mesh, irregular mesh and custom networks. First, a unified model combining scheduling and mapping is introduced using mixed integer linear programming (MILP). Task scheduling and core mapping have a significant impact on the overall performance of network on chip (NOC). Then, a novel graph model is proposed to consider the network irregularity and estimate communication energy and latency, since the number of network hops is not accurate enough for irregular mesh and custom networks. To enable this MILP modeling on irregular and custom NOC, a novel graph model called Labeled Graph is developed to calculate the communication latency and energy. Moreover, this model does not introduce any new variables, which makes our unified model as easy as a single scheduling algorithm in terms of the number of variables in MILP [9].

G. A new Buffer less routing algorithm:
A new buffer less routing algorithm that can be coupled with any topology is proposed. In the deep submicron regime, the power and area consumed by router buffers in network-on-chip (NoC) have become a primary concern. With buffers elimination, bufferless routing is emerging as a promising solution to provide power-and-area efficiency for NoC. The routing algorithm here is based on the concept of making-a-stop (MaS), aiming to deadlock and livelock freedom in wormhole-switched NoC, which enables in-order delivery without large buffering requirements at receiver side while maintaining the energy efficient. Compared to recent proposed deflecting bufferless routing BLESS-Worm, MaS reduces the increasing buffering requirements at receiver side which is caused by out-of-order arriving [10].

H. Low-Cost Router Micro architecture:
A low-cost, on-chip network router microarchitecture is proposed, which is different from the commonly assumed baseline router microarchitecture. It is to reduce the cost of on-chip networks by partitioning the crossbar, prioritizing packets in flight to simplify arbitration, and reducing the amount of buffers. By introducing intermediate buffers to decouple the routing in the x and the y dimensions, high performance can be achieved with the proposed, low-cost router micro architecture. By removing the complexity of a baseline router micro architecture, the low-cost router micro architecture can also approach the ideal latency in on-chip networks. However, the prioritized switch arbitration simplifies the router but creates starvation for some nodes. By eliminating the amount of buffers, simplifying the switch arbitration, and using dimension-sliced router micro architecture, a low-cost router micro architecture is developed that can provide single-cycle router latency and approach ideal on-chip network latency. To support a scalable 2D mesh network, they have introduced intermediate buffers internal to the router to decouple the two dimensions of the dimension-sliced router. By giving priority in switch arbitration to packets continuing to travel in the same dimension, the router pipeline delay is also minimized and reduces network contention to provide high throughput with limited amount of buffers. However, simplified switch arbitration causes starvation. The low-cost router used here does not include the many functionalities that have been proposed for on-chip networks, including fault tolerance, QoS, support for different traffic classes, and alternative routing algorithms [11].

I. A Low-Latency Source Synchronous Bypass NoC Architecture:
WaveSync is low-latency focused network-on chip architecture for globally-asynchronous locally-synchronous (GALS) designs. WaveSync facilitates low-latency communication leveraging the source-synchronous clock sent with the data, to time components in the downstream routers data-path to reduce the number of synchronizations needed. WaveSync accomplishes this by partitioning the router components at each node into different clock-domains; each synchronized with one of the orthogonal incoming source synchronous clocks in a GALS 2D mesh network. The data and clock subsequently propagate through each node router, synchronously, until the destination is reached, regardless of the number of hops it may take. As long as the data travel in the path of clock propagation, and no congestion is encountered, it will be propagated without latching, as if in a long-combinatorial path, with both the clock and the data accruing delay at the same rate. In a typical GALS NoC, each incoming link contains a source synchronous clock signal, which is used to synchronize the incoming data into the local clock domain/node. By contrast, WaveSync uses incoming clocks to time the routing components, eliminating the need for synchronization between the incoming data and the local node (i.e., PE) assuming no turns are needed. Synchronization can be further eliminated between the incoming data and the PE if the incoming link is the designated clock source for the PE [12].

J. Express Virtual Channels:
An express virtual channels (EVCs) is proposed to close the gap between the state of-the-art packet-switched network and the ideal interconnect, a novel flow control mechanism which allows packets to virtually bypass intermediate routers along their path in a completely non-speculative fashion, thereby lowering the energy/delay towards that of a dedicated wire while simultaneously approaching ideal throughput with a practical design suitable for on-chip networks. Although the multiplexing of network channels over multiple packet flows in packet-switched on-chip network designs leads to throughput gains, this comes with a significant latency, energy and area overhead in the form of complex routers. Here, they targeted this overhead in an attempt to approach the ideal interconnection fabric of dedicated wires between all nodes. An EVCs proposed, a novel flow control and router microarchitecture design, which use virtual lanes in the network to allow packets to bypass nodes along their path in a non-speculative fashion

and, hence, significantly reduce delay and energy consumption. The virtual paths created by EVCs also help lower the level of contention in the network, thereby allowing the network to push through more packets before saturation and, hence, improve throughput. Since network nodes are virtually connected using existing physical channels, EVCs improve performance with a negligible wiring area overhead and minimal hardware complexity. We presented a detailed microarchitecture for EVCs, analyzing the hardware and pipeline complexity of each of its components. A detailed evaluation, using both synthetic and actual workloads, showed EVCs significantly improving network energy, delay and throughput as compared to a state-of-the-art packet-switched network, and closely approaching the ideal interconnect [13].

K. Regular Reconfigurable Topology for Chip Multiprocessors:

It proposes an on-chip network with regular reconfigurable topology (RROCN). On-chip network is a promising solution for the on-chip communication problem of large-scale CMPs and a major factor in the performance, area, and power consumption of the overall system. The RROCN is a reconfigurable and hybrid communication structure contained routed network with 2D mesh topology and shared bus. The reconfiguration is implemented by disabling and bypassing the unwanted nodes of routed network and then organizing them as shared buses. To achieve this goal, a constructive algorithm, reconfiguration scheme, and modified XY routing algorithm with self-adaptive feature are proposed. With the constructive algorithm and reconfiguration scheme, the topology of RROCN could be configured into any 2D mesh topology under constrains of the original topology at runtime. The modified XY routing algorithm is also proposed to guarantee a packet can reach its destination. The RROCN is composed of shared bus and routed network. It is a hybrid scheme and thus takes advantages from both worlds. It is evaluated the RROCN with four specific reconfiguration topologies and compared them with a regular on-chip network. For an application with specific throughput demand, the RROCN could be configured with a topology that provides suitable throughput with less power consumption and lower zero-load latency. Furthermore, for acquiring lower latency, the RROCN could be configured with a topology that provides sufficient throughput to make the network non-congested. For acquiring less power consumption, the RROCN could be configured with a topology with less reconfiguration nodes. Due to the reconfiguration ability, the RROCN could be reconfigured for the optimization purpose in throughput, latency or power consumption or for finding the compromise between throughput, latency and power consumption. Therefore, the RROCN is a flexible scheme for chip-multiprocessors [14].

L. The Turn Model for Adaptive Routing:

It presents a model for designing wormhole routing algorithms that are deadlock free, livelock free, minimal or non-minimal, and maximally adaptive. A unique feature of this model is that it is not based on adding physical or virtual channels to network topologies (though it can be applied to networks with extra channels). Instead, the model is based on analyzing the directions in which packets can turn in a network and the cycles that the turns can form. Prohibiting just enough turns to break all of the cycles produces routing algorithms that are deadlock free, livelock free, minimal or non-minimal, and maximally adaptive for the network. It focuses on the two most common network topologies for wormhole routing, n-dimensional meshes and k-ary n-cubes, without extra channels. In an n-dimensional mesh, just a quarter of the turns must be prohibited to prevent deadlock. The remaining three quarters of the turns permit partial adaptiveness in routing. Partially adaptive routing algorithms are described for 2D meshes, n-dimensional meshes, k-ary n-cubes, and hypercubes. Its goal has been to make the best use of the channels in wormhole-routed interconnection net works. Deadlock freedom and livelock freedom are essentiaf for routing algorithms. Adaptiveness increases the chances that packets can avoid hot spots and faulty hardware and decreases the chances of indefinite postponement and livelock. Nonminimal routing allows, even greater hotspot avoidance and fault tolerance. The turn model, unlike other approaches to design adaptive routing algorithms, is applicable to networks with only the channels required by the network topologies (as well as to networks with extra physicaf or virtual channels). Applied to n-dimensional meshes and k-ary n-cubes without extra chanuels, the turn model produces several new, partially adaptive routing algorithms. While the turn model has many advantages, it also has some disadvantages. Adaptive routing can require more complex control logic for route selection than does nonadaptive routing, and this may increase node delay. Part of the complexity is due to the need for a router to decide between multiple output channels, all of which lead to the destination. Another part of the complexity is due to the need for a router to base the route selection on more header information. For dimension-order routing, a router typically bases a selection on the distance remaining in one of the dimensions. For adaptive routing, a, router must base a selection on the distance remaining in more than one, or all, dimensions. Every extra bit of header information that is required for the router to select an output channel increases router storage requirements and makes communication latencies more like those of store and forward [15].

III. PROPOSED HYBRID SCHEME BASED ON VIRTUAL CIRCUIT SWITCHING

In order to support VCS, PS, and CS connections at the same time, modified router architecture with five ports is proposed, as shown in Fig. 1. Compared with the baseline router, the additional hardware of the proposed router includes the bypass path, the circuit configuration, and the VCS state. First, the bypass path is added in each input unit for allowing flits to go directly to the crossbar switch. Second, each input unit contains a PS state and a VCS state. The PS state corresponds to the VC state of the baseline PS router, and the VCS state is used to support VCS connections [3]. Third, the circuit configuration unit is to store the interconnect information for CS connections. In this paper,

both the PS and the VCS states have *n* fields corresponding to *n* VCs. In addition, these *n* VCs are shared by VCS connections and PS connections. Information of the VC in the downstream router is stored in the VCS state to denote which downstream VC is connected to the corresponding VC. Incoming flits can directly traverse the crossbar switch according to the corresponding field of VCS state.

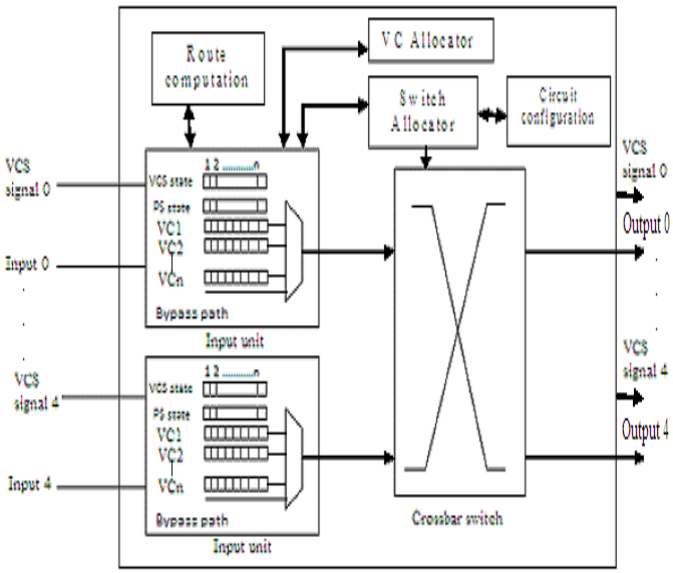

Fig. 1. Architecture of the router [3].

The VCS signal is used to preconfigure the crossbar switch for VCS connections. It can be transmitted simultaneously with the transmission of flits. The VCS signal is $(\log 2\ n + 1)$-bit wide, including a VC identifier and a flag for representing its validity. The VCS signal does not traverse the crossbar switch, but is generated by the router. It is output when the crossbar switch just completes the configuration for the VCS connection during the SA stage. The overhead caused by VCS signal can be negligible. First, the VCS signal is only issued when crossbar switches of the VCS connection wait to be preconfigured. Due to the low activity of VCS signal, the power overhead caused by VCS signal can be much less than the power saving by bypassing buffer writing, routing, and arbitration of routers. Second, in the network with two VCs, the width of VCS signal is 2 bits. Moreover, the proposed router architecture has been implemented in Verilog HDL and synthesized using Spartan 3 FPGA. As for the data overhead, since route information can be stored in the VCS state and circuit configuration, packets on VCS and CS connections do not need route information. However, packets on PS connections need route information in the data of head flit [3].

IV. CONCLUSION

This paper shows the various switching techniques, routing algorithms and different router architectures in order to minimize latency, power and other routing constraints on NoC. A hybrid scheme called virtual circuit switching, which optimizes both communication latency and power is proposed.

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