International Journal For Technological Research In Engineering
Volume 2, Issue 7, March-2015 *ISSN (Online): 2347 - 4718*

ON-CHIP POWER MANAGEMENT BY DIGITAL PWM

Nivedhitha. M
PG Scholar, Department of ECE, T.J.Institute of Technology
Chennai – 600 097

Abstract: The digital PWM modulator circuit is capable of varying the duty cycle of the output (PWM) according to the digital input word. A digitally controlled current starved pulse width modulator is described. The current from the power grid to the ring oscillator is controlled by a header circuit. By changing the header current, the pulse width of the switching signal generated at the output of the ring oscillator is dynamically controlled, permitting the duty cycle to vary between 25% and 90%. A duty cycle to voltage converter is used to ensure the accuracy of the system under process, voltage and temperature (PVT) variations. A ring oscillator with two header circuits is proposed to control both duty cycle and frequency of the operation. Analytic closed form expressions for the operation of a PWM are provided. The proposed PWM is appropriate for dynamic voltage scaling systems due to the small on-chip area and high accuracy under PVT variations. The header circuit controls the amount of current delivered to the pMOS transistors within the ring oscillator. This header circuit provides a high granularity duty cycle. It provides a duty cycle in constant frequency. Here digital to analog converter using digital pulse width modulator is designed.
Index Terms: Current starvation, digital-controlled oscillators, pulse width modulation, ring oscillators.

I. INTRODUCTION

Voltage controlled oscillators (VCOs) are widely used to generate a switching signal where certain characteristics of this signal can be controlled. Two types of VCOs are primarily used in high performance integrated circuits (ICs), inductor-capacitor (LC) oscillators, and ring oscillators. LC oscillators can operate at high frequencies and exhibit superior noise performance. Alternatively, ring oscillators occupy significantly smaller on-chip area with a wider tuning range. Due to these advantages, ring oscillators have found widespread use in modern ICs . A conventional ring oscillator consists of an odd number of inverters where the output of the last inverter is fed back to the input of the first inverter. The delay provided by each inverter in this chain produces a phase shift in the switching signal. The sum of these individual delays (i.e., phase shifts) and the feedback from the last to the first inverter produces a total phase shift of 2π that causes the circuit to oscillate. The frequency of this oscillation depends upon the sum of the inverter delays within the chain. The duty cycle of the generated switching signal is typically 50% for conventional ring oscillators where the pMOS and nMOS transistors within the inverters provide the same rise and fall transition times. The duty cycle of a ring oscillator can be tuned by controlling the transition time of the inverters within the ring oscillator. Header and footer circuits are widely used to control the current supplied to the pMOS and nMOS transistors within the ring oscillator inverter chain. Although the header and footer circuits are typically used to control the frequency, these circuits can also control the duty cycle of a ring oscillator. Here, a digitally controlled pulse width modulator (PWM) comprised of a header circuit, ring oscillator, and duty cycle to voltage (DC2V) converter is described. The duty cycle of the PWM is determined from proposed closed form expressions, yielding a simple dependence on the header current. The high accuracy of the proposed expressions is confirmed by simulation results. The header circuit controls the amount of current delivered to the pMOS transistors within the ring oscillator. Contrary to conventional header circuits, where the header is connected to all of the inverters within the ring oscillator chain, the proposed header circuit is connected to every other inverter stage to dynamically control the pulse width of the output signal. This header circuit provides a high granularity duty cycle control with a step size of 2% of the period. An additional header circuit regulates the supply current delivered to the remaining inverter stages, providing improved control while maintaining a constant switching frequency. Additionally, a DC2V converter, based on the frequency to voltage converter proposed, maintains the accuracy of the PWM under process, voltage, and temperature (PVT) variations. Under PVT variations, the maximum change in duty cycle is less than 2.7% of the period. Owing to the small on-chip area, fast control circuitry, high accuracy under PVT variations, and dynamic duty cycle and frequency control governed by accurate closed-form expression, the proposed PWM is an effective circuit to dynamically change the duty cycle of the input switching signal for on-chip voltage regulators. This circuit enables high granularity dynamic voltage scaling at runtime and reduces the response time from milliseconds to nanoseconds. The proposed PWM architecture is described where the working principle of the header circuitry and DC2V converter is explained, and the analytic expressions for the proposed PWM timing parameters are provided. The functionality and accuracy of the proposed circuit under PVT variations are validated with predictive technology models at the 22-nm technology node. The voltage-controlled oscillator (VCO) is a commonly investigated circuit due to its use in phase-locked loops (PLLs) and clock and data recovery circuits (CDRs). The architecture of the VCO falls into two main categories: the ring oscillator and the LC oscillator. Although LC oscillators have superior phase noise performance compared to ring oscillators, ring oscillators still have numerous advantages. They generally require a relatively small area and can be more easily integrated with

digital CMOS circuits, reducing cost. Also, they have a wider tuning range than LC oscillators, making them more robust over process and temperature variations. Despite its widespread usage, the ring oscillator still poses difficulties when it comes to design, analysis and modeling. The design of a voltage-controlled oscillator involves many trade-offs in terms of speed, power, area and application domain. For the designer to make informed decisions regarding these trade-offs, an accurate method to determine the frequency of oscillation of the VCO is necessary. One way to determine the oscillation frequency is to simulate the circuit using a numerical simulator, such as hspice. Although the oscillation frequency predicted may be accurate for the exact circuit simulated, there is no clear way for the designer to know how to improve the circuit. The designer does not know which circuit elements are controlling the oscillation frequency, and the effect design changes will have. The designer can find some basic trends by running hundreds of different simulations, but even then, the effect of each part of the circuit may not be clear. An alternative method of design is to generate an analytical equation for the oscillation frequency of the VCO. An analytical equation will contain terms based on circuit and process parameters. The circuit parameters can show the designer what trade-offs are possible based on design changes. The process parameter components of the equation can be used to determine the limits of the VCO for a given technology. This can be very important if a VCO with a high oscillation frequency is required, or if the designer wishes to determine how the frequency limits of the VCO will change with scaling. The ring oscillator is a crucial component that has been widely used in analog and digital applications due to its compact design, wide tuning range, and low power consumption. These characteristics make ring oscillators attractive for applications with extremely stringent power and cost budget. Despite its popularity, the ring oscillator suffers from poor frequency accuracy, as its center frequency can vary as much as 26% from chip to chip. This not only limits the ring oscillator's application as a frequency reference in systems with tight frequency accuracy specifications, but also leads to over-design in other parts of the system to accommodate the worst frequency offset of the oscillator. A case in point would be the frequency reference of the wake-up radio in wireless sensor networks (WSN). This application requires small, cheap, and power-efficient components, which should be an ideal application for a ring oscillator. Unfortunately, its accuracy requirement of a few percent is beyond what can be easily achieved with conventional ring oscillators. With the rapid development of portable devices, the demand of high performance conflicting with the requirements of long running times and battery life. As a result, high conversion efficiency has become the key property for the power management of battery powered equipment. Since the load changes with time, the conversion efficiency should be kept high enough over a wide range of load current. Switching mode power supplies with PWM control are widely used due to their high efficiency. However, switching loss is the dominating loss and efficiency will decrease when a heavy load is supplied. PSM control maintains high efficiency at a light load by minimizing the switching frequency in order to reduce switching loss. Digitally controlled power converters are becoming more and more competitive than their analog rivals due to their inherent advantages, such as being programmable for different applications, robustness with noise and process variation, and the convenience of implementing advanced control schemes.

II. ON-CHIP POWER MANAGEMENT

The mainstay of the project is to design and analyze digital pulse width modulator. To increase the on chip power management and also the performance of the circuit. In the proposed design a Digital to analog converter using DPWM and Low pass Filter. The Proposed system consists of Digital controlled oscillators, a synchronous counter, a combinational reset and a combinational comparison logic. we are replacing VCO through DCO to design Digital pulse width modulator. DCO designed by flip flop. DCO act as the register. DCO tunable strength is high comparing VCO. It stored the input word. Digital to analog converter designed by the digital pulse width modulator and low pass filter.

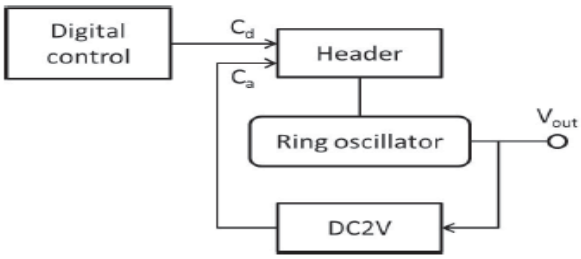

Fig. 1. Proposed PWM

A. Header Circuit

An addition based current source, has been proposed. This circuit is used, as a header to compensate for temperature and process variations by maintaining a constant current to the ring oscillator. Note that this header circuit has one input voltage that controls the gate voltage of M1 and M2. By controlling this gate voltage, the sum of the current is maintained constant over a wide range of temperature and process variations. Alternatively, in this paper, a modified version of this header circuit, is introduced to control the duty cycle by changing the transition time of the pMOS transistors at every other inverter stage within the ring oscillator.

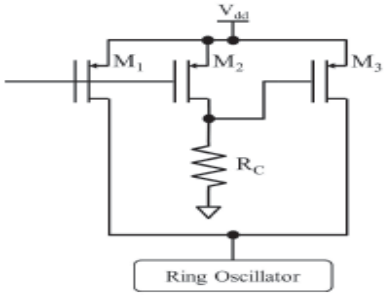

Fig. 2. Addition based current source as header circuit

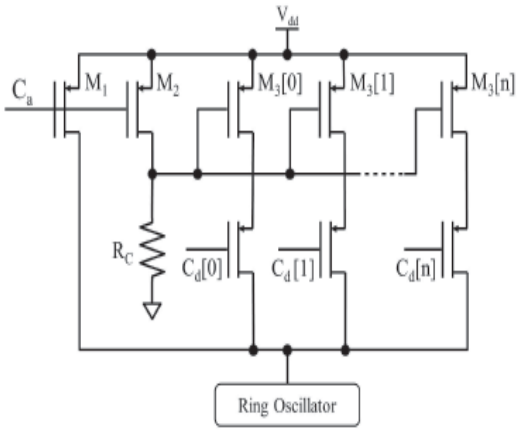

Fig. 3. Parallel pMOS transistors

Gates *M*1 and *M*2 are controlled by the analog signal *Ca*. As opposed to a single transistor *M*3 whose gate is connected to a resistor, as shown in Fig.3, multiple parallel pMOS transistors *M*3[0 : *n*] are added in place of *M*3 in the proposed header circuit. The pMOS transistors are designed with increasing device size and individually tuned to provide both increased dynamic range and dynamic control of the duty cycle with 2% increments. All of these transistors have the same gate-to-source voltage, but the voltage at the drain terminals is controlled by other switch transistors. Additional pMOS transistors are connected in series with these transistors as switch transistors. The gate voltage of these switch transistors is controlled by a digital controller that turns on (and off) the individual header stages through control signals *Cd* [0 : *n*]. Turning on the entire header stages produces the maximum current to the ring oscillator, which in turn minimizes the duty cycle. The variations in the leakage current are more prominent when the device size is small. To mitigate these variations, larger than minimum size transistors are used in sub-65-nm technology nodes. The first two transistors in the header circuit (*M*1 and *M*2) are therefore comparably large to minimize any mismatches. A minimum channel length of 150 nm is used for these two input transistors as opposed to 40 nm for the other transistors.

B. Duty Cycle to Voltage Converter

The frequency to voltage converter proposed is used as a DC2V converter. A circuit schematic of this DC2V converter is shown

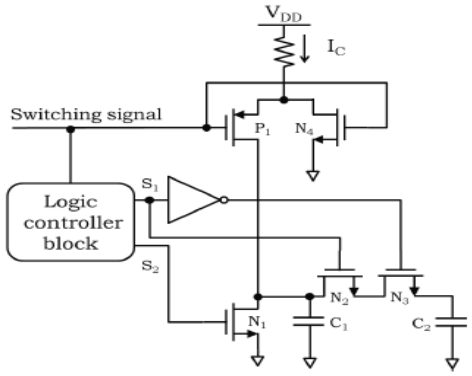

Fig. 4. DC2V Converter

There are primarily three different phases of this circuit. During the first phase, capacitor *C*1 is charged through transistor *P*1. In the second phase, transistors (i.e., switches) *N*2 and *N*3 are turned on to allow charge sharing between *C*1 and *C*2. During the last phase, *C*1 is discharged through *N*1. The charge time of *C*1 depends upon the duty cycle of the input switching signal. A signal with a greater duty cycle causes more charge to accumulate on *C*1, increasing the output voltage of the DC2V converter. The proposed DC2V converter controls the bias current from the header circuitry through negative feedback, mitigating PVT variations. Intuitively, when the header current is reduced, the duty cycle of the ring oscillator is greater, increasing the output voltage of the DC2V converter. As a result, the voltage at the gate of the M2 transistor increases and the current IC through resistor *R* decreases, pulling down the gate voltage of the active header stages. Thus, the current flow through the header to the ring oscillator is increased, compensating for the original reduction in current. A more complete explanation of the working principles of this circuit as well as the logic controller block is available.

C. On-Chip Implementation Issues

On-chip implementation requirements are efficient, small, inexpensive, and simple regulator topologies that besides providing constant and well regulated voltage should also be capable of allowing the creation of multiple voltage islands on-chip. This is important given the technology trend towards system-on-chip and chip multiprocessors. Some of the challenges include:

• Efficiency degradation due to size reduction of filter components and high switching frequencies.

• Smaller capacitor provides less charge to the load, which becomes vulnerable to large di/dt events that cause voltage fluctuations.

• In order to reduce fluctuations, decoupling capacitors are used but with the overhead of increasing chip area.

• On-chip regulator uses the filter capacitor for both decoupling and filtering, which causes large voltage droops since large load current steps rapidly drain out the limited charge stored on the capacitor.

• Circuit droops are assisted by filter component size reduction.

• Inductance issues. A decrease in inductance size results not only in faster switching and higher inductor ripple current, but in a more noticeable parasitic inductance in the circuit as well.

• Inductor fabrication challenges.

D. Pulse Width Modulation

The duty cycle of the switching regulator is modulated by pulse width modulation in order to control the amount of power sent to the load. It measures the output voltage and when it is lower than the desired voltage of 3.7V it turns on the switch. When output voltage increases above 3.7V, PWM turns off the switch. The desired output voltage is realized by switching voltage to the load with the appropriate duty cycle. Since VIN is 3.7V and VOUT is 1.8V then duty

cycle is 1.8V/3.7V=0.486. The step-down occurring is relatively small, from 3.7V to 1.8V, therefore the operating duty cycle of the regulator is sufficient to maintain high regulator efficiency. On the other hand, if the step-down was bigger, such as from 10V to 1.8V, then duty cycle would be 1.8V/10V= .180, which is very small and makes it difficult to design a voltage regulator with high efficiency. In addition, duty cycle is also dependent on ton, which is 1.94us, and period, T, which is 4us. So, efficiency of the regulator varies with duty cycle. An extreme duty cycle challenges the design of an efficient regulator.

III. MODULAR DESCRIPTION

A. Replacement of VCO by DCO

VCO is replaced by DCO. The DCO is designed using flip flop and it acts as the register. DCO has high tunable strength when comparing with VCO. It stores the input word. Each bit has one flip flop.

B. Design of Combinational Comparison Logic

Combinational comparison logic designed by basic gates. Asynchronous counter is designed. The counter is incremented at every clock (CLK) cycle. We will use the combinational comparison logic in AND gate and XOR gate. It takes the DCO output as the input.

C. Design and Analysis of DPWM

The Digital controlled oscillators, a synchronous counter, a combinational reset and combinational comparison logic are integrated. It generates duty cycle in various percentage and at constant frequency.

D. Design of DAC

The Digital to Analog Converter Using Digital Pulse Width Modulator, Low pass filter is designed. The complex programmable logic device is used for analysis of performance in area, delay and power.

IV. SIMULATION

A seven stage ring oscillator is described in this paper to provide a switching signal with a wide duty cycle range. The proposed circuit is designed in a 22-nm CMOS predictive technology model (PTM). Certain parameters in the technology model file are modified to include process corners such as typical-typical (TT), slow-slow (SS), fast-fast (FF), fast-slow (FS), and slow-fast (SF). Simulation results characterizing the accuracy of the proposed PWM for different duty cycle ratios under PVT variations. The effect of the bias current on the duty cycle of the ring oscillator output is discussed without constraints on the period of the output signal under a constant period constraint.

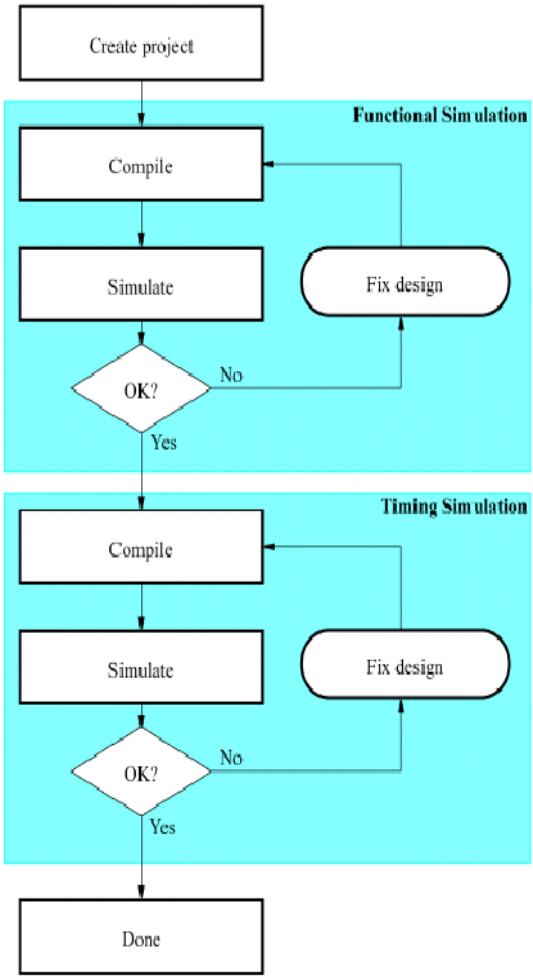

Fig. 5. Simulation flow

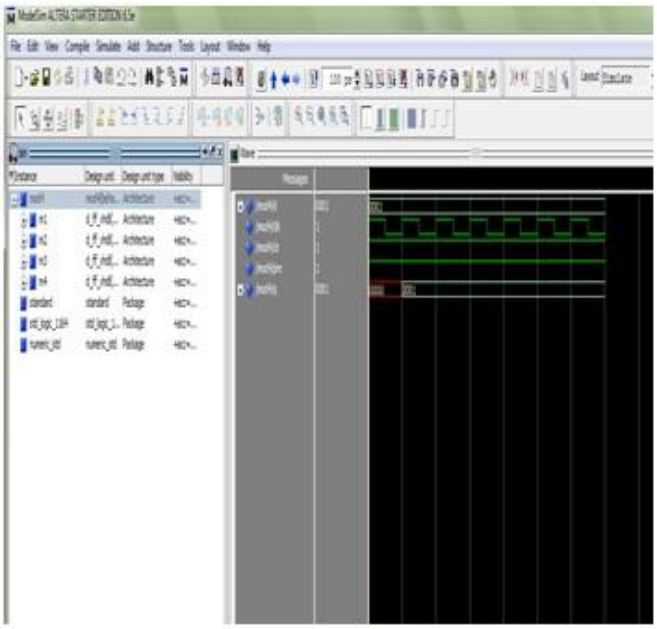

Fig.6. Simulation Output For Combinational Comparison Logic And Counter

V. CONCLUSION

The scaling of minimum feature sizes down to nanometer range and the spiraling frequencies in GHz scale has lead to system-on-a-chip (SOC) implementation for many emerging applications. Power consumption has a critical impact on IC performance, and therefore, its management is important. Ineffective power management causes lower chip performance, increases area and makes the design nonfunctional. Therefore, more than ever, power integrity is vital in the successful design of today's electronic systems. Here by replacing VCO by DCO, the digital signals helps in giving more accurate results with high granularity. Small on-chip area and dynamic duty cycle control can be achieved.

REFERENCES

[1] B. H. Calhoun and A. Chandrakasan, "Ultra-dynamic voltage scaling using sub-threshold operation and local voltage dithering in 90 nm CMOS," in Proc. IEEE ISSCC, Feb. 2005, pp. 300–599.
[2] Digital Pulse-Width Modulation Control in Power Electronic Circuits, Angel V. Peterchev A.B. (Harvard University) 1999 M.S. (University of California, Berkeley) 200
[3] S. Kose, I. Vaisband, and E. G. Friedman, "Digitally controlled wide range pulse width modulator for on-chip power supplies," in Proc. IEEE ISCAS, May 2013, pp. 2251–2254.
[4] High Performance Power Distribution Networks with On-Chip Decoupling Capacitors for Nanoscale Integrated Circuits, Mikhail Popovich, University of Rochester,Rochester, New York ,2007
[5] On-Chip Voltage Regulation for Power Management in System-on-Chip, Juliana Gjanci, B.S University of Illinois at Chicago, 2006
[6] B. Razavi, Design of Analog CMOS Integrated Circuits. New York, NY, USA: McGraw-Hill, 2001.
[7] T. D. Burd, T. A. Pering, A. J. Stratakos, and R. W. Brodersen, "A dynamic voltage scaled microprocessor system," IEEE J. Solid-State Circuits, vol. 35, no. 11, pp. 1571–1580, Nov. 2000.
[8] R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Kose, and E. G. Friedman, Power Distribution Networks with On-Chip Decoupling Capacitors, 2nd ed. New York, NY, USA: Springer-Verlag, 2011.
[9] S. Kose, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "Active filter based hybrid on-chip Dc–Dc converters for point-of-load voltagemregulation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 4, pp. 680–691, Apr. 2013.
[10] S. Docking and M. Sachdev, "A method to derive an equation for the oscillation frequency of a ring oscillator," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 50, no. 2, pp. 259-264, Feb. 2003.
[11] W. Kolodziejski, S. Kuta, and J. Jasielski, "Current controlled delay line elements' improvement study," in Proc. ICSES, Sep. 2012, pp. 1–4.

