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HARMONIC MITIGATION IN CASCADE MULTILEVEL INVERTER FOR DEVELOPED H-BRIDGE USING GENETIC ALGORITHM

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Abstract: ***This paper presents the developed H-Bridge for harmonic minimization in a cascade multilevel inverter. The main objective of SHEPWM Technique is used to produce low switching losses, then it means it produce lower order harmonics by solving non linear equation with the fundamental component is satisfied .In this paper ,the GA is applied to a 15 level inverter for solving the equation. such as the genetic algorithm (GA), have been used with success to compute optimal switching angles for multilevel inverters with many dc sources while minimizing several lower order harmonics.***

Index Terms: Cascade Multi Level Inverter, Developed H - Bridge, Genetic Algorithm(GA), Bee Algorithm(BA) SHE PWM and Voltage Source Inverter(VSI).

I. INTRODUCTION

Today there are many applications for multilevel inverters, such as flexible ac transmission system (FACTS) equipment, high voltage direct current lines and electrical drives. There are three conventional structures for multilevel inverters: diode-clamped, flying capacitor and cascaded multilevel inverter with separate dc sources. The cascaded multilevel inverter is composed of a number of single-phase H-bridge inverters and is classified into symmetric and asymmetric groups based on the magnitude of dc voltage sources. In the symmetric types, the magnitudes of the dc volt-age sources of all H-bridges are equal while in the asymmetric types, the values of the dc voltage sources of all H-bridges are different. The major advantage of this paper and its algorithms is related to its ability to generate a considerable number of output voltage levels by using a low number of dc voltage sources and power switches but the high variety in the magnitude of dc voltage sources is their most remarkable disadvantage. In order to increase the number of output voltage levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of cascaded multilevel inverters is proposed. It is important to note that in the proposed method ,the unidirectional power switches are used. Then, to determine the magnitude of the dc voltage sources, a new algorithm is proposed. Moreover, the proposed method is compared with other method from different points of view such as the number of MOSFETs, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch. Finally, the performance of the proposed method in generating all voltage levels through a 15-level inverter is confirmed by simulation using MATLab. The main advantage of all these structures is the low variety of dc voltage sources, which is one of the most important features in determining the cost of the inverter. The main disadvantage of this structure is related to its bidirectional power switches and the total cost of the inverter.

II. CASCADE MULTILEVEL INVERTER

The cascaded multilevel inverter consists of a series of H-bridge inverter units. In this method, the objective is elimination of low-order harmonics, while the fundamental harmonic is satisfied. Thus the cascaded multilevel inverter can be reduce the Total Harmonic Distortion(THD) using the control of switching angle i.e. Conduction angle control method. A Unlike the diode clamped or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors. As shown in Fig.1,the proposed topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six unidirectional power switches (Sa, Sb, SL,1, SL,2, SR,1, and SR,2) and two dc voltage sources (VL,1 and VR,1). In this paper, these topologies are called developed H-bridge. As shown in Fig. 1, the simultaneous turn-on of SL,1 and SL,2 (or SR,1 and SR,2) causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided. In addition, Sa and Sb should not turn on, simultaneously.

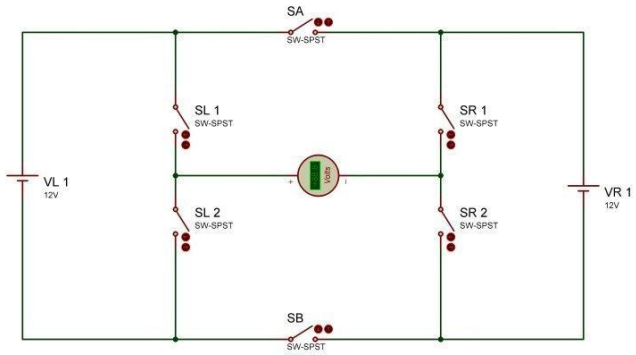

Fig. 1. Proposed seven-level inverter

Each full-bridge can generate three different voltage outputs: +Vdc, 0, and −Vdc. However, all three multilevel inverters can produce staircase waveform as shown in Fig.1 .The number of output phase voltage levels i n a cascaded multilevel inverter is 2N + 1, where N is the number of dc sources. For example, phase voltage waveform for a 7-level cascaded multilevel inverter with three isolated dc sources

(N = 3) is shown in Fig. 1. Each H-bridge unit generates a quasi-square waveform by phase-shifting the switching timings of its positive and negative phase legs. The cascaded H-bridge inverters having more no of advantages such as modular structure compare to other method ,such a structure and less number of components, it is one of the topologies has high power rating with reduced THD and switching losses. The asymmetric MLI reduces the number of input DC sources required and increases the number of levels in the output. The modulation strategy used for reducing the THD is the selective harmonic elimination PWM technique. The SHE PWM strategy has also been used in multilevel inverters. The features for cascade multilevel inverter such as Voltage regulation, VARcompensation,3 Harmonicfiltering in power systems, Device voltage sharing is automatic, CMI has smaller dv/dt compared to series connected 2-level inverter.

TABLE I
Output Voltages of the Proposed Seven-Level Inverters

No	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	Sa	Sb	Vo
1	1	0	0	1	0	1	VL.1
2	1	0	0	1	1	0	-VR,1
3	1	0	1	0	0	1	VL,1+VR,1
4	1	0	1	0	1	0	0
	0	1	0	1	0	1	0
5	0	1	1	0	1	0	-VL,1
6	0	1	1	0	0	1	VR,1
7	0	1	0	1	1	0	-VL,1 -VR,1

A. Selective Harmonic Elimination PWM

A 7-level inverter waveform shown in Fig. 2 has three variables θ1, θ2 , and θ3 , where Vdc1, Vdc2, and Vdc3 are assumed to be equal. Considering equal amplitude of all dc sources, the Fourier series expansion of the output voltage waveform, shown in Fig. 2, will be written as

$(wt) = \sum\infty\ 1\ VnSin(n\omega t)$…….( )

where Vn is the amplitude of the nth harmonic. Switching angles are limited between zero and $\pi/2$ ($0 \leq \theta i < \pi/2$). Because of odd quarter-wave symmetric characteristic, harmonics with even order become zero. The objective of SHEPWM is to eliminate the lower order harmonics while remaining harmonics are removed with filter. In this paper, without loss of generality, a 7,15-level inverter is chosen as a case study to eliminate its low-order harmonics. SHE PWM technique uses many mathematical methods to eliminate specific harmonics such as 5th, 7th, 11th, and 13th harmonics. The popular Selective Harmonic Elimination method is also called fundamental switching frequency based on harmonic elimination Theory.

III. GENETIC ALGORITHM

Genetic algorithm is a computational model that solves optimization problems by imitating genetic processes and the theory of evolution by using genetic operators like reproduction, crossover, mutation etc. Amounts of applications have benefited from the utilization of genetic algorithm. Genetic algorithm is still a novel technique for PWM-SHE technique.

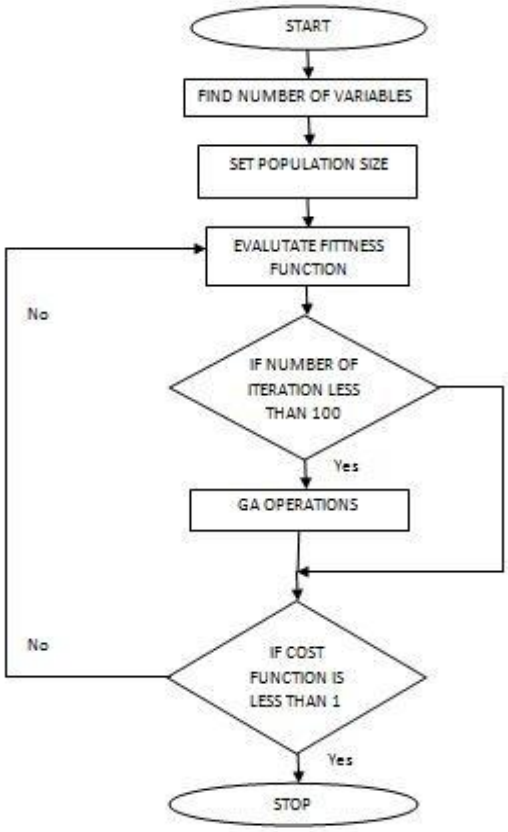

Fig. 2 Flowchart of Genetic Algorithm

A. Reproduction

The reproduction operator determines how the parents are chosen to create the offspring. This operator is a process in which chromosomes are copied according to their objective function values i.e. the degree of conformity of each object is calculated and an individual is reformed under a flat rule depending on the degree of conformity.

B. Crossover

Crossover is the most significant operation in GA. It creates a group of children from the parents by exchanging genes among them. The new offspring contain mixed genes from both parents. By doing this, the crossover operator not only provides new points for further testing within the chromosomes, which are already represented in the population, but also introduces representation of new chromosomes into the population to allow further evaluation on parameter optimization.

C. Mutation

Mutation is another vital operation. It works after crossover operation. In this operation, there is a probability that each gene may become mutated when the genes are being copied from the parents to the offspring. This process is repeated, until the preferred optimum of the objective function is reached.

D. Evaluation of fitness function

The most vital item for the GA to evaluate the fitness of each chromosome is the cost function. The purpose of this study is to minimize specified harmonics; therefore the fitness function has to be associated to THD. In this work the fifth, seventh, eleventh, and thirteenth harmonics at the output of an fifteen -level inverter are to be minimized.

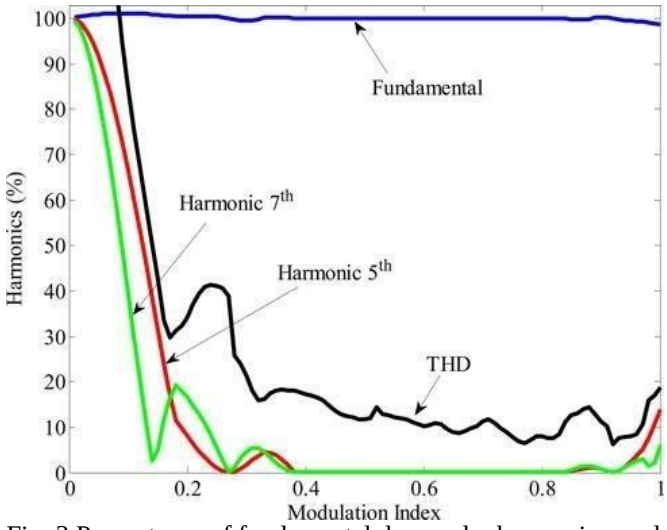

Fig. 3 Percentages of fundamental, low-order harmonics, and THD.

Fig.3, 4 show the situation of switching angles, harmonic conditions, CDF and THD versus M . Line voltage THD is calculated by an accurate method, presented .If a region has a low fitness function, all low-order harmonics are maintained close to 0. For other ranges, the value of harmonics is significant so the equations cannot be solved. In both states, because of penalty, considered in fitness function, the fundamental harmonic is near the desired value. Reduction in value of low-order harmonics leads to a decrease in THD value. To show the effectiveness of GA, BA is employed as a reference. For comparison, BA with the same GA parameters is implemented. The parameters of both algorithms are shown in Table II. GA codes have more complexity and running time in comparison with BA. In fact, this complexity implies greater running time. Although GA has more complexity and run time, in GA the probability of reaching to global minima for all run number run is more greater

TABLE II: COMPARISON OF PARAMETERS BETWEEN BA AND GA

PARAMETERS	GA	BA
Population Size	100	100
Number of iteration in each run	200	200
Number of runs	1,2,5,10	1,2,5,10
Running time	100 sec	700 sec
Code complexity	moderate	low
Probability of reach to global minima	high	moderate

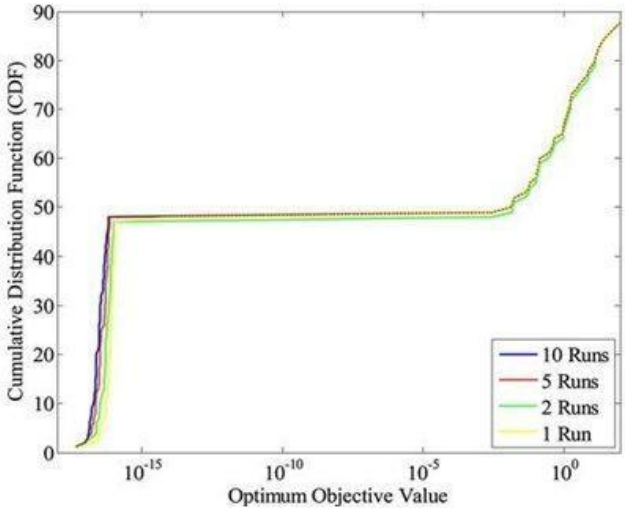

Fig.4 CDF curve obtained by GA.

IV. SIMULATION RESULTS

From the simulation results using genetic algorithm, it is clear that for 7,15-Level cascaded multilevel inverter the 5th, 7th, 11th and 13th harmonics and for 15-Level inverter 5th, 7th, and 11th harmonics and their magnitudes are negligible relatively to the fundamental component. Fig.5,6 shows the simulation results for the output voltage waveform of 7,15-level inverter. Fig.7, 8 shows the THD value of proposed 7,15-level inverter .

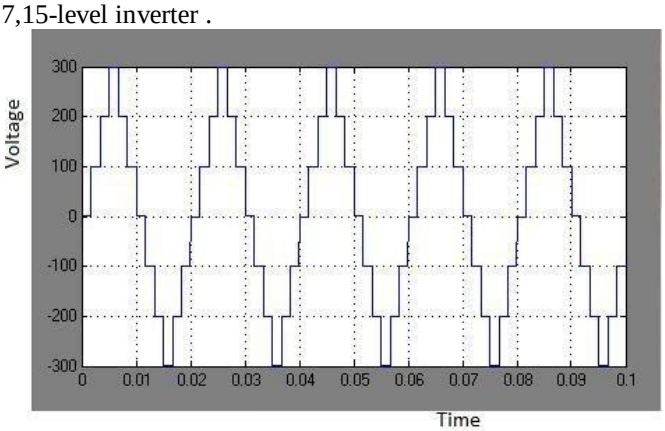

Fig.5 Output Voltage Waveform of Proposed Sevel-Level Inverter

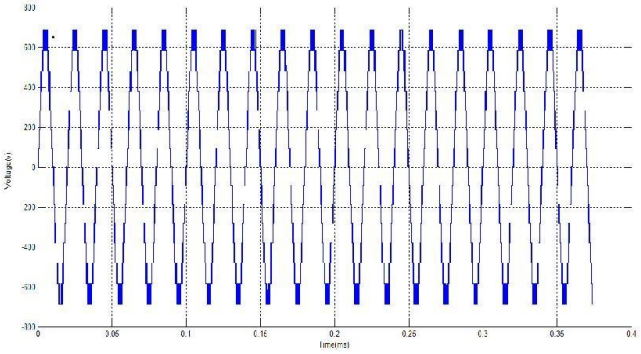

Fig.6. Output Voltage Waveform of Proposed Fifteen-Level Inverter

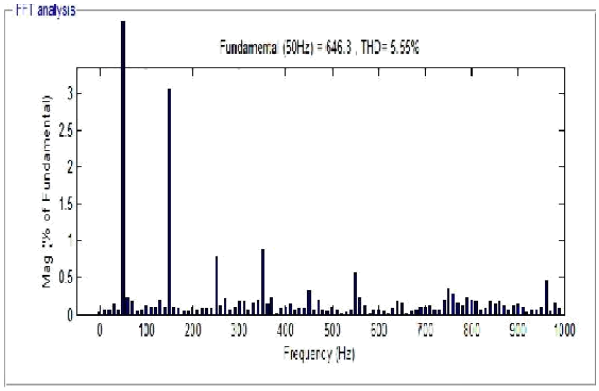

Fig.7 THD Value of Proposed Seven- Level Inverter

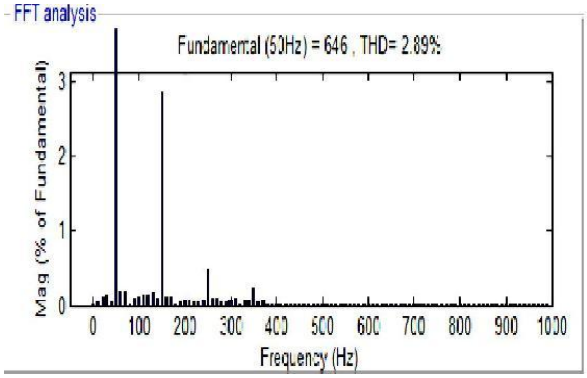

Fig.8 THD Value of Proposed Fifteen –Level Inverter

V. CONCLUSION

In this paper, elimination of low-order harmonics using SHEPWM strategy is investigated In addition, a new algorithm to determine the magnitude of the dc voltage sources has been proposed. According to the comparison results, the proposed topology requires a lesser number of MOSFETs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional method. However, the proposed Method has a higher number of varieties of dc voltage sources in comparison with the others. The performance accuracy of the proposed method was verified through the MATLab version 2011a simulation results.

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