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IMPLEMENTATION OF POSITIVE LOGIC TWO STEP BOOST CONVERTER BASED ON PV ARRAYS SYSTEM

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Abstract: An energy-efficient maximum power point tracking (MPPT) circuit with a fast-tracking time for use with 800-µW PV energy harvesters is presented in this paper. The proposed MPPT circuit uses a successive approximation register MPPT algorithm, which has a power down mode and a fast tracking time, to achieve low power consumption and energy savings. The prototype MPPT circuit, which consists of analog-based circuits, has been implemented and fabricated in a 0.35-µm BCDMOS process. The MPPT core occupies an area of 3 mm2 and consumes 4.6 Mw of power. The tracking time is reduced by 69.4% and the stored energy is increased by 31.4% as compared to the conventional hill climbing-based MPPT algorithm under indoor conditions.

Index Terms: Energy harvesting, maximum power point tracking (MPPT), photovoltaic (PV), solar cell, wireless sensor networks (WSNs).

I. INTRODUCTION

Renewable energy sources are alternatives to our conventional energy sources such as fossil fuels e.g. oil, coal, gas that is not renewable. The conventional energy sources are limited and can be exhausted. Many renewable energy sources such as solar, wind, biomass, hydro, geothermal and ocean power exist. Among PV has the advantage of clean and no pollution, and etc. So, PV systems are attracting attention in the world. The basic element of a PV system is the solar cell .A solar cell directly converts the energy of sunlight directly into electricity in the form of dc. A typical PV cell consists of a p-n junction formed in a semiconductor material similar to a diode. Solar photovoltaic (PV) electricity generation is not available and sometimes less available depending on the time of the day and the weather conditions. Solar PV electricity output is also highly sensitive to shading. When even a small portion of a cell, module, or array is shaded, while the remainder is in sunlight, the output falls dramatically. Therefore, solar PV electricity output significantly varies. From an energy source standpoint, a stable energy source and an energy source that can be dispatched at the request are desired. As a result, energy storage such as batteries and fuel cells for solar PV systems has drawn significant attention and the demand of energy storage for solar PV systems has been dramatically increased, since, with energy storage, a solar PV system becomes a stable energy source and it can be dispatched at the request, which results in improving the performance and the value of solar PV systems. There are different options for integrating energy storage into a utility-scale solar PV system. Specifically, energy storage can be integrated into the either ac or dc side of the solar PV power conversion systems which may consist of multiple conversion stages. Every integration solution has its advantages and disadvantages.

Different integration solutions can be compared with regard to the number of power stages, efficiency, storage system flexibility, control complexity, etc. An energy-efficient maximum power point tracking (MPPT) circuit with a fast-tracking time for use with 800-Mw PV, energy harvesters is presented. The proposed MPPT circuit uses a successive approximation register MPPT algorithm, to achieve low power consumption and energy savings. The prototype MPPT circuit, which consists of analog-based circuits, has been implemented and fabricated in a 0.35-µm BCDMOS process. Photovoltaic (PV) cells, which convert solar irradiation directly into electrical energy, have been widely utilized as the energy harvesters in applications such as wireless sensor networks (WSNs), autonomous systems, and power plant systems. However, there are several challenges to energy harvesting with PV cells. Furthermore, the maximum output power from a PV cell degrades under changing atmospheric conditions. To maximize the efficiency of the PV energy harvester, a maximum power point tracking (MPPT) technique, which enables the operating point of the PV cells to track the maximum power point (MPP), has been implemented in the PV energy harvesters.

II. DESIGN CONSIDERATIONS

The efficiency of the energy harvester, including the PV cell, heavily depends upon the conditions of solar irradiance. This section quantifies and analyzes the irradiance variation in the measured datasets. In addition, the effectiveness of the power down mode in the PV energy harvester is examined under the measured irradiance conditions. Since a perpetual MPPT operation under small irradiance variation wastes a portion of the energy of the several hundreds of microwatts of the PV energy harvester, the power down mode during the MPPT operation is a possible solution to minimize the energy loss in the MPPT circuit.

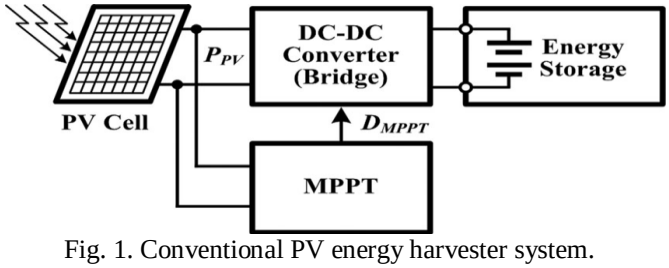

Fig. 1. Conventional PV energy harvester system.

A. Variability of Solar Irradiance on the PV Cell

Several previous studies regarding the variability of solar irradiance analyzed a dataset of irradiance at a sampling period of 1-h, 1-min, or 1-s. However, since the time constant of the PV cell, which represents the dynamic time response of the PV cell, is considerably faster, this work uses a fast sampled dataset of solar irradiance to allow precise analysis. The sampling period used to measure the changes in the solar irradiance is 10 μs or faster for our target PV cell, which has a time constant of 20 μs. Fig. 2(a) shows the measured datasets for an irradiation G with a sampling period of 2.5 μs. The measured irradiance, which includes noise components, is slowly changed in comparison with the sampling period. Fig. 2(b) depicts the probability density function of the irradiance that has the largest irradiance variation in Fig. 2(a), at various sampling interval Δt. As Δt increases, the standard deviation σ, which represents the diversity of the irradiance during Δt, also increases. Due to the relative standard deviation σ/G less than 1% at a Δt of 50 ms, a representative value of irradiance Gi can be defined as the mean value of the irradiance during the period Δt of 50 ms. A variation in irradiance can be represented by the irradiance increments ΔG for aΔt of 50 ms, as shown in Fig. 2(c). Here,ΔG = Gi+1−Gi . Gi+1 and Gi are two consecutive irradiances with a time interval of Δt. Fig. 2(d) shows the frequency distribution function of the irradiance increments F(ΔG), which classifies ΔG according to the number of times that the irradiance changes of ΔG occur.

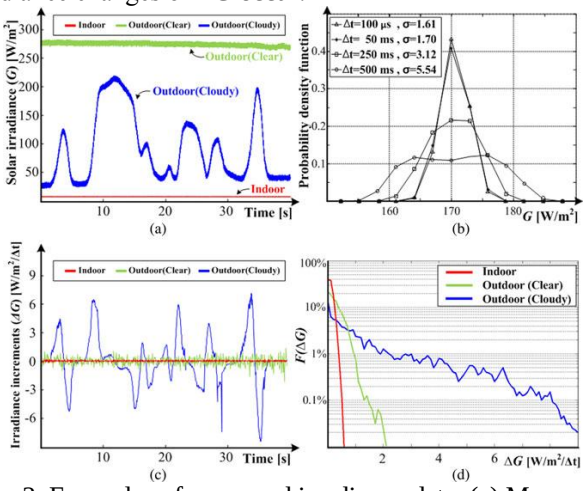

Fig. 2. Examples of measured irradiance data. (a) Measured data with 400k Samples/s. (b) Probability density function of the largest irradiance variation part in (a) with various time intervals Δt. (c) Irradiance increments with Δt of 50 ms. (d) Frequency distribution function of irradiance increments.

B. Power down Mode in MPPT

The irradiance variability can be modeled as a ramp signal, which has an amplitude of ΔGi , and the probability of the ramp signal F(ΔGi) · N with a period of Δt = 50 ms, as shown in Fig. 3(a). Here, N is the total number of cycles of the ramp signal over a period of T. F(ΔGi) · N refers to how frequently the ramp irradiance signal with the amplitude of ΔGi occurs during a period of T. Fig. 3(b) shows the operation of the MPPT with the power down mode under the conditions of the highlighted irradiance variation. In the active mode, the MPPT circuit is turned ON and the PV output power PPV tracks the MPP. The MPP tracking should be performed within the active mode time TON. In the power down mode, the MPPT circuit turns OFF and keeps the load impedance of the PV cell during the power down mode time TOFF. Although PPV has a small change in the power down mode, this analysis does not consider the variation of PPV during power down mode, since this quantity of variation is small compared to the generated energy level of a PV cell.

The energy delivered by the PV cell to the energy storage EStore is given by

$$EStore = EPV - EMPPT = \int PPV(t)dt \quad \int PMPPT(t)dt \quad (1)$$

where PPV is the power produced by the PV cell and PMPPT is the power consumed by the MPPT circuit. In (1), the energy loss in the dc–dc converter is neglected. There is an optimal power down mode time that minimizes energy loss in the MPPT circuit. TOFF = 42, 15.5, and 34.5 ms are the optimal values for indoor conditions, cloudy outdoor conditions, and clear outdoor conditions, respectively. The power down mode increases the value of EStore by 32%, 12%, and 4% under the indoor, cloudy outdoor and clear outdoor conditions, respectively.

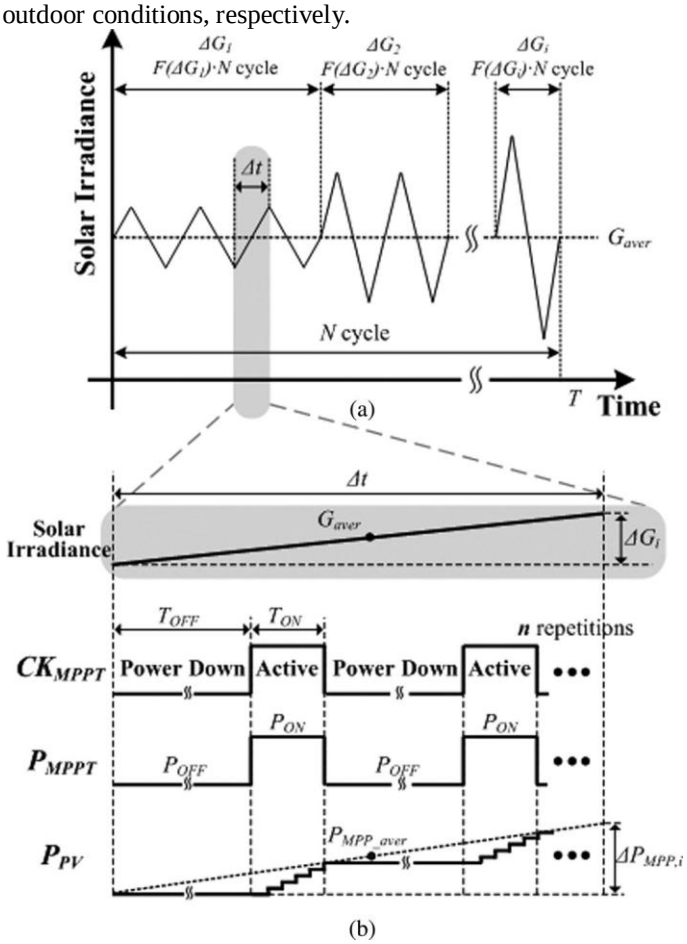

Fig. 3. (a) Modeling of irradiance variation. (b) Timing diagram of MPPT operation with power down mode.

III. PROPOSED PV ENERGY HARVESTERS

A. SAR MPPT Algorithm

The selection of the optimal value of TOFF for the power down mode is critical to reduce the energy consumed by the MPPT circuit. However, because the MPPT operation is suspended when the system is in the power down mode, the operating point of the PV cell is different from the ideal MPP at the beginning of the active mode. To reduce waste of the energy delivered in the active mode, a short TON is required. Moreover, a short TON results in additional energy savings for the MPPT circuit. Fig. 4 presents a flow diagram of the proposed SAR MPPT algorithm with a fast MPPT time, which can reduce TON. This algorithm is a hill climbing algorithm with SAR operation. The SARMPPT determines the direction of perturbation of DMPPT, which represents the operating point of the PV cell, using the binary search method of successive approximation. If the value of DMPPT increases, the operating point moves in such a direction that the output voltage of the PV cell is decreased. Assume that a 4-bit DMPPT is used in the MPPT operation; it begins by comparing the output power of the PV cell [PPV(t – 1)] at DMPPT = 1000 and PPV(t) at DMPPT = 1001. PPV(t) and PPV(t – 1) represent the PV output power of the current state and the previous state, respectively. If PPV(t) > PPV(t – 1), the duty control bits, which determine the next states [PPV(t + 1) and PPV(t + 2)], are set to DMPPT = 1100 and DMPPT = 1101. In contrast, if PPV(t) < PPV(t – 1), the duty control bits of the next states are DMPPT = 0100 and DMPPT = 0101. This SAR operation starts to decide the MSB bit to an LSB bit. After the completion of the SAR operation, the operating point of the PV cell is located at the MPP and the system enters the power down mode. In the power down mode, the proposed algorithm maintains the final value of DMPPT and the other operations are suspended, which results in no power consumption in the MPPT circuit during the power down mode. The tracking time of the MPPT algorithm is the required time to reach the MPP, when the irradiance changes. It can be represented by the MPPT operation cycles. Let us assume that an N-bit DMPPT is used in the MPPT operations. The conventional hill climbing algorithm works like an N-bit digital counter and needs additional 4 cycles to confirm that the PV output power reaches the MPP. Therefore, the conventional hill climbing algorithm requires 2N +4 cycles to reach the MPP in the worst case, whereas the proposed SARMPPT algorithm requires 2N –1 cycles to reach the MPP. In this case, the step size of the conventional hill climbing algorithm is equal to the smallest step size of the SAR MPPT algorithm. Fig. 5 shows ideal power tracking graphs for the conventional hill climbing algorithm (4 bit) and the proposed SAR MPPT algorithm (4 bit), and compares their MPPT algorithm during only active mode (for further details, see the Appendix). The proposed SAR MPPT algorithm achieves a fast tracking time, no oscillations around the MPP. Furthermore, the enhancement of the MPPT efficiency during active mode improves the entire MPPT tracking efficiency.

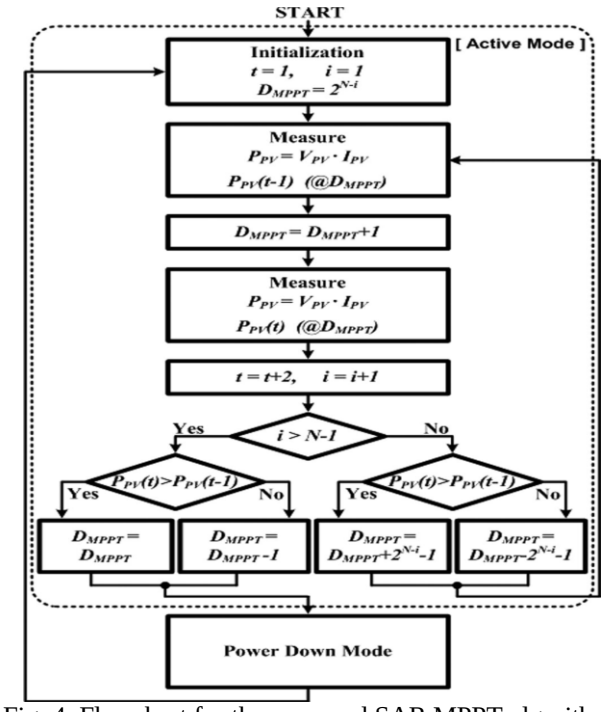

Fig. 4. Flowchart for the proposed SAR MPPT algorithm.

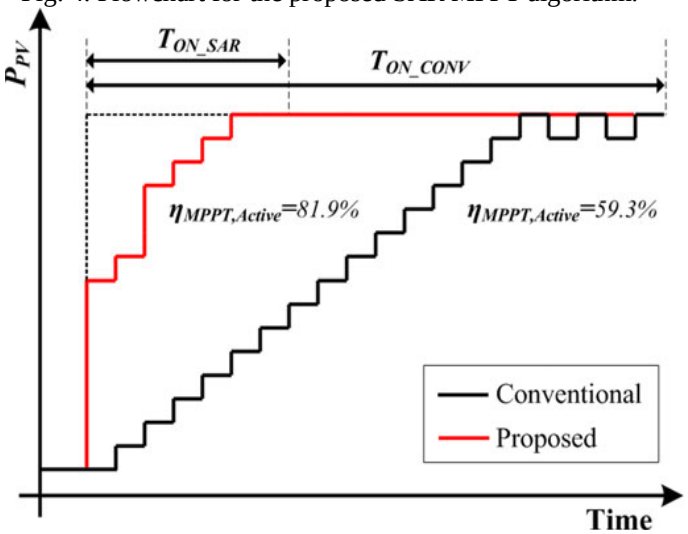

Fig. 5. Performance comparison graphs between the conventional hill climbing (4 bit) and the proposed SAR MPPT algorithms (4 bit) in the active mode.

B. Circuit Description

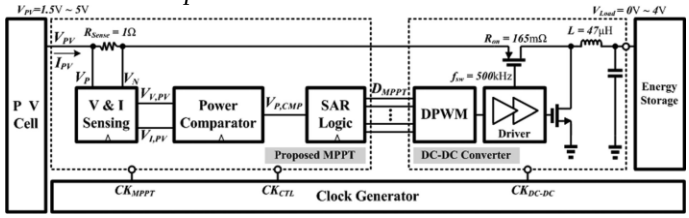

Fig. 6. Block diagram of the proposed MPPT circuit for a solar energy harvester.

Fig. 6 shows a block diagram of the proposed MPPT circuit for WSN PV energy harvesters. The PV energy harvester consists of an MPPT circuit, a dc–dc converter, a clock generator, and energy storage. The dc–dc converter utilizes

the conventional buck-type converter with an external inductor and a digital pulse width modulator. The clock generator produces system clock signals for execution of the proposed SAR MPPT algorithm. To achieve low power consumption, the MPPT circuit, which operates according to the proposed SAR MPPT algorithm, is implemented with an analog-based voltage-and current sensing circuit, a power comparator circuit, and SAR logic circuits. The voltage-and-current sensing circuit is implemented using a switched-capacitor integrator circuit, as shown in Fig. 8(a). Here, the two-phase clocks of PH1 and PH2 are non-overlapping. If PH1 = High, *C*1 and *C*3 sample the current and voltage of the PV cell at a sensing resistor *R*Sense, respectively. If PH2 = High, the amplifier integrates the output current *I*PV and voltage *V*PV of the PV cell. The switched-capacitor integrator reduces the effects of the fluctuation of *VP* and *VN*. In addition, the common-mode input voltage of the amplifier maintained as a constant, which improves the linearity of the amplifier gain.

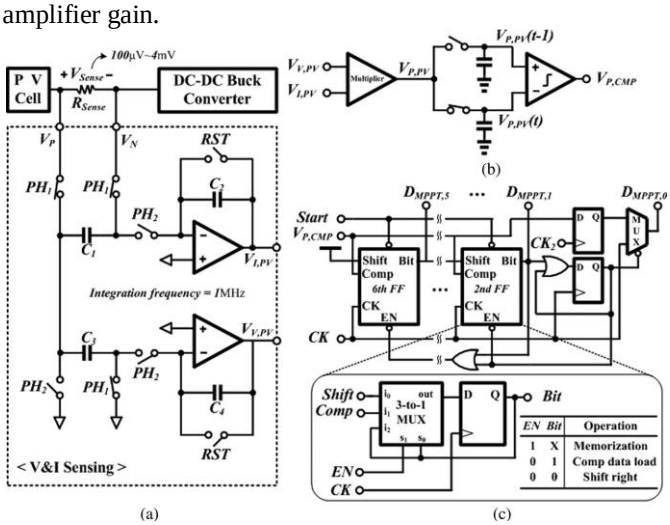

Fig. 7. Circuit diagrams of (a) voltage-and-current sensing, (b) power comparator, and (c) 6-bit SAR logic.

The power comparator circuit is illustrated in Fig. 7(b). The multiplier circuit is implemented using the conventional analog multiplier of the Gilbert-cell. It calculates the output power of the PV cell using *VV*, *PV* and *VI* ,PV. The input voltage ranges of the Gilbert cell (*VV* ,PV and *VI* ,PV) are 400m*V*p-p .To compare the output power of the current state [*VP*,PV(*t*)] with the output power of the previous state [*VP*,PV(*t* – 1)], the sample-and-hold circuit and comparator are used. If *VP*,PV(*t*)>*VP*,PV(*t* – 1), the output of the power comparator *VP*,CMP becomes high. *VP*, CMP determines the direction of the next states in the SAR MPPT algorithm.

Fig. 7(c) presents a circuit diagram of the 6-bit SAR logic. To support the controlling of the LSB of *D*MPPT, a flip-flop and a multiplexer are added. In the active mode, the signal *Start* is set to high and *D*MPPT changes according to the SAR MPPT algorithm. In the power down mode, *D*MPPT is stored and the last value of the active mode is retained.

IV. EXPERIMENTAL RESULT

The proposed circuit was implemented and fabricated in a 0.35-μm BCDMOS process. The proposed MPPT circuit excluding the dc–dc converter occupies an area of 2000 μm × 1500 μm. The buck-type dc–dc converter with external inductor of 47 μH is used. The switching frequency of the dc–dc converter is 500 kHz and Ron of the switches is 165 mΩ. The experimental environment of the PV energy harvester is shown in Fig. 10. A 1000-Whalogen lamp was used instead of solar irradiance. An a-Si PV cell with an open-circuit voltage of 5 V and short-circuit current of 30 mA at 1000 W/m2 was used.

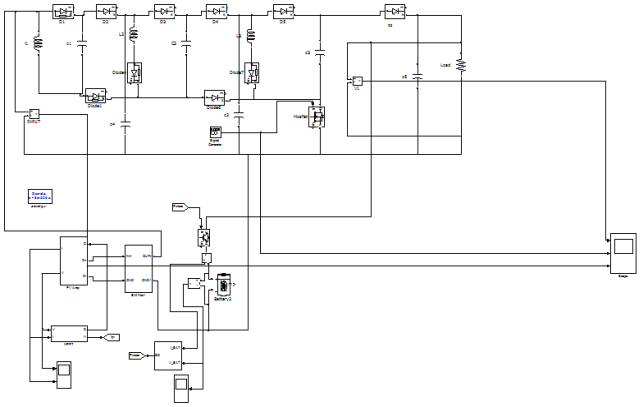

Fig.8. Simulation model of two step positive voltage of pv module

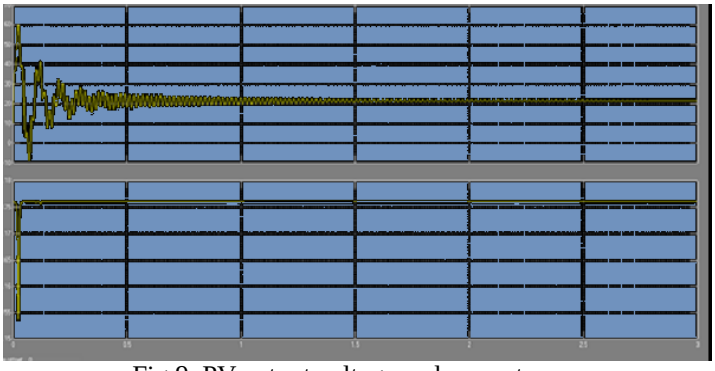

Fig.9. PV output voltage and current

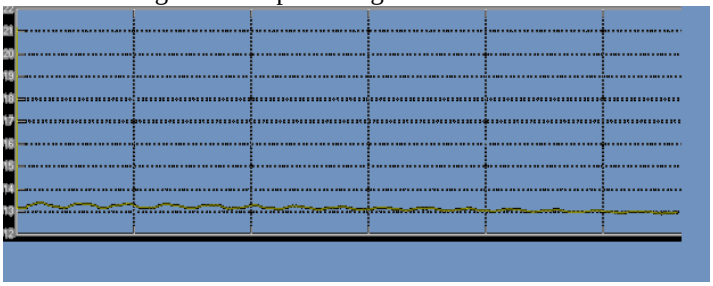

Fig.10. PV output of Battery voltage

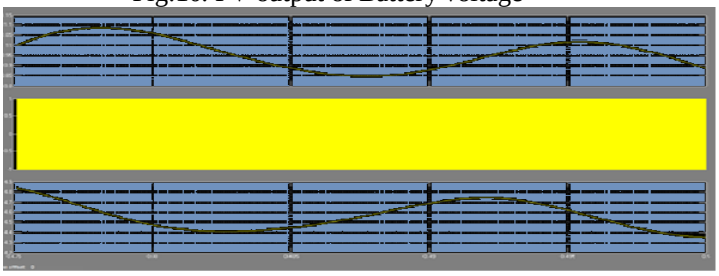

Fig.11. Input waveform of PV module

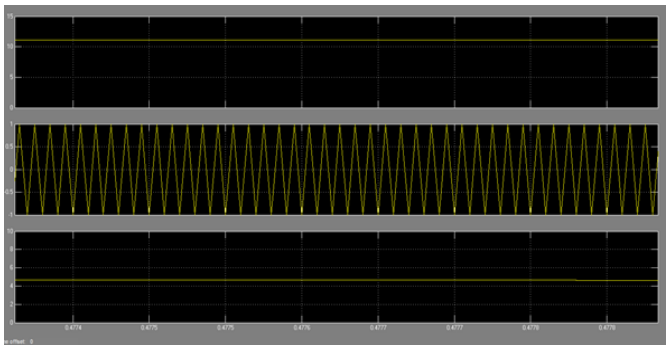

Fig.12. waveform of output voltage of two step positive voltage with PV module.

V. CONCLUSION

The two step positive voltage boost converter based MPPT with PV array has been implemented. The proposed INC MPPT algorithm is extensible and applicable to high power application. The proposed circuit has sufficiently high energy efficient for use as the PV energy harvester. Further the regulation is high, Higher efficiency and improved life. DC boost converter and a Maximum power point tracker to optimize efficiency at all times.INC Conductance algorithm has been slightly more efficient and has reached to the MPP in a shorter time period.

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