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NAND-BASED DIGITALLY CONTROLLED DELAY-LINES

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Abstract: The Combinational circuit which we designed was NAND-based digitally controlled delay-lines (DCDL) present a glitching problem which may limit their employ in many applications. This paper presents a glitch-free NAND-based DCDL which overcame this limitation by opening the employ of NAND-based DCDLs in a wide range of applications. The proposed NAND-based DCDL maintains the same resolution and minimum delay of previously proposed NAND-based DCDL. The theoretical demonstration of the glitch-free operation of proposed DCDL is also derived in the paper. Following this analysis, three driving circuits for the delay control-bits are also proposed. Proposed DCDLs have been designed in a 90-nm CMOS technology and compared, in this technology, to the state-of-the-art. Simulation results show that novel circuits result in the lowest resolution, with a little worsening of the minimum delay with respect to the previously proposed DCDL with the lowest delay. Simulations also confirm the correctness of developed glitching model and sizing strategy. As example application, proposed DCDL is used to realize an All-digital spread-spectrum clock generator (SSCG). The employ of proposed DCDL in this circuit allows to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state inverter based DCDLs.

Index Terms: All-digital delay-locked loop (ADDLL), all-digital phase-locked loop (ADPLL), delay-line, digitally controlled oscillator (DCO), flip-flops, sense amplifier, spread-spectrum clock generator (SSCG).

I. INTRODUCTION

In recent deep-sub micrometer CMOS processes, time-domain resolution of a digital signal is becoming higher than voltage resolution of analog signals. This claim is nowadays pushing toward a new circuit design paradigm in which the traditional analog signal processing is expected to be progressively substituted by the processing of times in the digital domain. Within this novel paradigm, digitally controlled delay lines (DCDL) should play the role of digital-to-analog inverters in traditional, analog-intensive, circuits. From a more practical point of view, nowadays, DCDLs are a key block in a number of applications, like all-digital PLL (ADPLL), all-digital DLL (ADDLL), all-digital spread-spectrum clock generators (SSCGs), and ultra-wide band (UWB) receivers with ranging feature. The "classical" approach to design a DCDL is using a delay-cells chain and a MUX to select the desired cell output. In these Mux-based DCDLs, the MUX delay increases with the increase of the number of cells. This results in a tradeoff between the delay range and minimum delay of the DCDL. It is worth to note that is a critical design parameter in much application. As an example in ADPLL/ADDLL, determines the maximum output frequency of the circuit. This property remains true also for the All-digital SSCG, where a correct DCDL synchronization is obtained only by imposing that is lower than one half input clock period. The large of MUX-based DCDLs can be reduced by using a tree-based multiplexer topology. This however results in an irregular structure which complicates layout design and, consequently, also increases the nonlinearity of the DCDL. The DCDL topology uses again a delay cells chain. Differently from the above approaches, in this technique each cell is constructed by using NAND gates. This apparently solves the tradeoff related to the MUX of previous structures. A deepen analysis of the structure, however, reveals that the input capacitance of the DCDL increases linearly with the number of cells. This, clearly, reintroduces a tradeoff between the number of cells and the minimum delay, similarly to MUX-based DCDLs. A similar reasoning applies also to the MUX-based DCDL is constructed by using a regular cascade of equal delay elements (DE). In this circuit, the multiplexer of previous DCDL is conceptually spread among all cells. In this way the minimum delay is very low and becomes independent of the number of cells. In addition the highly regular topology allows a simple layout organization which provides very low nonlinearity layout effects. Each DE is constructed by using only NAND gates, obtaining a very good linearity and resolution. An analysis of the circuit reveals that the DCDL resolution is given by (being the delay of a NAND gate). The DCDL uses again a structure of cascaded delay elements. Differently each element is constructed y using three-state inverters (TINV), obtaining a resolution. Since the pull-up network of a TINV requires two series devices whereas a NAND gate uses a single device in the pull-up, we can expect that the resolution of this solution is higher than the resolution of NAND-based DCDLs. The DCDL is also based on a cascade of equal delay elements, which allows a simple layout organization. In this case each delay element is constructed by using an inverter and an inverting multiplexer. Glitching is a common design problem in systems employing DCDLs. In most common applications, DCDLs are employed to process clock signals; therefore a glitch-free operation is required. A necessary condition to avoid glitching is designing a DCDL which have no-glitch in presence of a delay control-code switching. This is an issue at the DCDL-design level. Many approaches are known to avoid glitching in Mux-based DCDLs. It is interesting to observe that the DCDL topologies of and from a logical point of view, correspond to distributed MUX-based structure. Glitching in these topologies can be avoided

by using a thermometer code for the control-bits. On the other hand the NAND-based DCDL topology presents a glitching problem that, to the best of our knowledge, is still not known in Literature. It is worth to note that in the ADDLL topologies of the DCDL glitching is filtered by the phase detector and harmonic locking circuitry during locking phase. In other applications, however, the presence of this glitching phenomenon can substantially limit the employ of NAND-based DCDLs. This represents a substantial drawback of this topology in comparison to the solutions. The errors that in some applications can originate from DCDL this paper gives two contributions to the design of NAND-based DCDLs. First it is shown and analyzed the glitching problem of the NAND-based DCDL. Afterwards a novel glitch-free NAND-based DCDL is presented. The proposed NAND-based DCDL allows achieving a resolution, similarly to the NAND-based DCDL The paper is organized as follows. These results are used to propose three different driving circuits for the delay control-bits of proposed DCDL. Simulation results for a 90-nm CMOS technology.

II. EXISTING NAND SYSTEM

The classical approach to design a DCDL is using a delay-cells chain and a MUX to select the desired cell output. In these mux-based DCDLs, the MUX delay increases with the increase of the number of cells. This results in a tradeoff between the delay range and minimum delay (tmin) of the DCDL. It is worth to note that tmin is a critical design parameter in many applications. In ADPLL/ADDLL, tmin determines the maximum output frequency of the circuit. This property remains true also for the All-digital SSCG , where a correct DCDL synchronization is obtained only by imposing that is lower than one half input clock period. Each element is constructed by using three-state inverters (TINV), obtaining a resolution. Since the pull-up network of a TINV require two series devices thereby increasing a minimum delay. The DCDL uses again a structure of cascaded delay elements. Differently, each element is constructed by using three-state inverters (TINV), obtaining a resolution tR = 2 tTINV Since the pull-up network of a TINV requires two series devices whereas a NAND gate uses a single device in the pull-up network. In next case each delay element is constructed by using an inverter and an inverting multiplexer, this topology creates two drawbacks first is due to the different delays of the inverter and the multiplexer which results in a mismatch between odd and even control-codes. Second drawback is due to the large multiplexer delay, which provides a resolution higher than the resolution of both NAND based DCDLs and TINV-based DCDLs. Drawbacks: Glitches, Tradeoff between delay range and minimum delay.

III. PROPOSED SYSTEM

Differently from the above approaches, in this technique each cell is constructed by using NAND gates. This apparently solves the tradeoffs related to the MUX of previous structures. A deepen analysis of the structure, however, reveals that the input capacitance of the DCDL increases linearly with the number of cells. This, clearly, reintroduces a trade-off between the number of cells and the minimum delay tmin, similarly to MUX-based DCDLs. The DCDL is constructed by using a regular cascade of equal delay elements (DE). In this circuit, the multiplexer of previous DCDL is conceptually spread among all cells. In this way the minimum delay is very low and becomes independent of the number of cells. In addition the highly regular topology allows a simple layout organization which provides very low nonlinearity layout effects. Each DE in is constructed by using only NAND gates, obtaining a very good linearity and resolution. The NAND gate uses a single device in the pull-up, we can expect that the resolution of this solution is higher than the resolution of NAND-based DCDL.

A. Proposed Technique

In the NAND-based DCDL, the circuit is composed by a series of equal delay-elements (DE), each composed by four NAND gates. The NAND based DCDL consists of the fast input of each NAND gate, dummy cells added for load balancing. The delay of the circuit is controlled through control-bits, which encode the delay control-code with a thermometric code. By using this encoding, each DE can be either in pass-state or in turn-state. In DCDL applications, to avoid DCDL output glitching, the switching of delay control-bits is synchronized with the switching of In input signal. Glitching is avoided if the control-bits arrival time is lower than the arrival time of the input signal of the first DE which switches from or to the turn-state. This condition is not sufficient to avoid glitching. In this circuit, in fact, it is possible to have output glitches also considering only the control-bits switching, with a stable input signal. Proposed System Advantages: Glitches free, Appropriate Synchronization

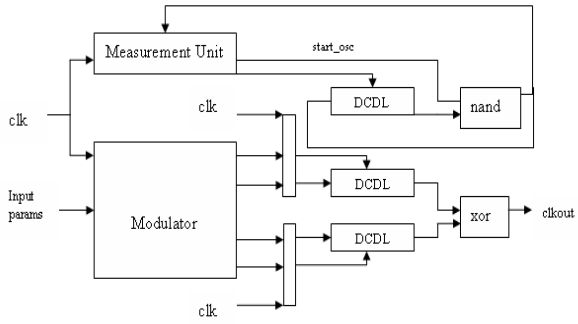

Fig. 1. Block Diagram of Proposed System

B. Design and Analysis of Delay Elements

In this module design and analyses the delay elements using NAND gates. Each element consists of four NAND gates. Delay elements will reduce the errors.

C. Design and Analysis of 64 Delay Elements

In this module, design and analyses the performance of delay elements. Each element having control word s and t. Clock frequency is varied by control word s and t.

D. Design and Analysis of Spread Spectrum Clock Generator (SSCG)

In this module, design and analyses the digital spread-spectrum clock generator (SSCG). The employ of proposed DCDL in this circuit allows reducing the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state Inverter based DCDLs.

TABLE I: Logic gates of each DE in Proposed DCDLs

S_j	T_j	DE state
0	1	*Pass*
1	1	*Turn*
1	0	*Post-Turn*

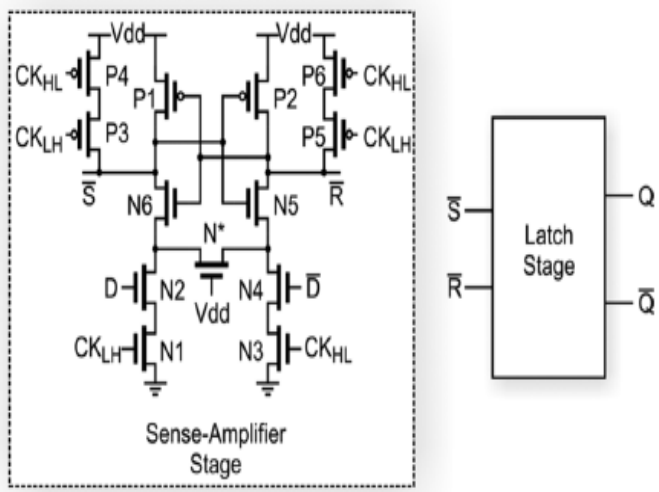

Fig. 2. Double-clock flip-flop realized by using a sense-amplifier-based topology.

IV. SIMULATION AND RESULTS

In order to verify the effectiveness of proposed solution, the circuits of Figs. 1–5 and the DCDL of [8] have been designed for a 90-nmCMOS technology, with 1.0Vsupply voltage and using standard-Vt devices. The considered length, for all DCDLs, is 64 elements. All NAND-based DCDLs have been sized in order to optimize t_R. All NAND gates present a ratio 2 W_P/W_N= 1.5, where W_P and W_N represent the widths of pMOS and nMOS, respectively. In proposed DCDL the INL is improved by slightly changing the ration W_P/W_N of NAND "3" in each DE. This NAND gate, in fact, presents opposite switching for odd and even delay control- codes and is, therefore, responsible for an asymmetry in the minimum delay between these two conditions. This asymmetry is the major contribution to the INL of NAND-based DCDL. Before evaluating the performances of the DCDLs, a series of simulations to verify the glitching behavior have been performed. To that purpose a simulation test bench has been considered in which the delay control-code is changed by using a test vector of 10 000 random delay control-codes. In these conditions, the circuit exhibited 5208 glitches.

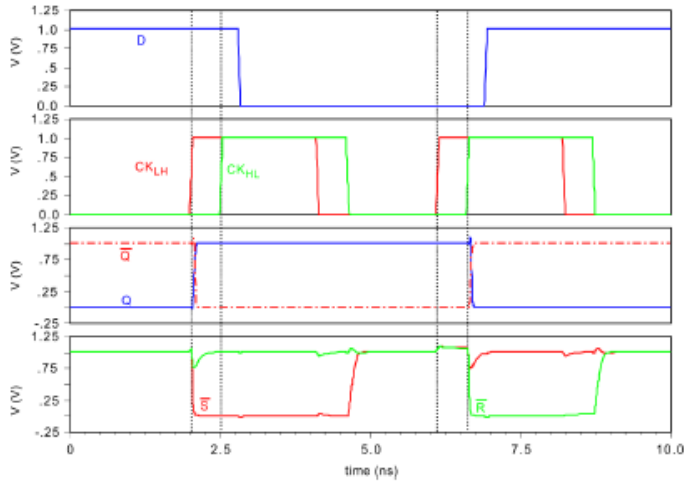

Fig. 3. Transient simulation of the flip-flop of Fig. 2.

The glitching behavior of proposed DCDL has been verified by considering the waveforms of Fig. 6, and by varying the two delays Δ_S and Δ_t. The obtained simulation results and comparison of the results with the two timing constraints is done. The graph presents on the two axis the delays Δ_S and Δ_t, normalized to the NAND gate propagation delay t_{NAND}. A circle and a cross are used to represent simulations in which either no glitching or a glitching behavior is observed, respectively.

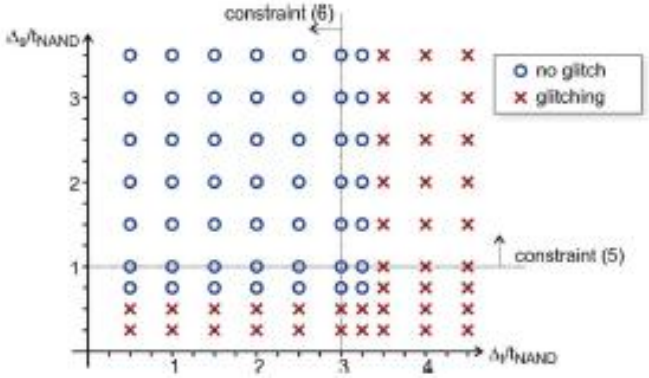

Fig. 4. Results of glitching simulations of proposed DCDL by varying Δ_S and Δ_S. The DCDL has been simulated with 10 000 random delay control-codes.

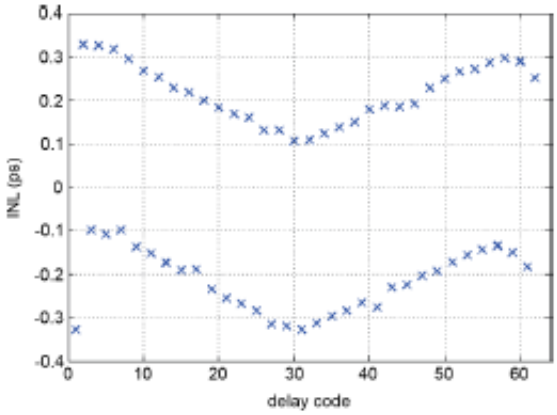

Fig. 5. Simulated INL of the proposed non-inverting DCDL in typical process corner.

TABLE II
DCDL PERFORMANCES FOR A 90-nm CMOS TECHNOLOGY (TYPICAL CORNER, 1.0 V, 27 °C)

	Glitch	t_R (ps)	t_{min} HL/LH (ps)	INL_{max} (ps)	norm. MOS count	P_D (μW/MHz)
NAND-based [12]-[15]	yes	48	49 46	0.7	1.0	0.92
TINV-based [8]	no	76	29 35	0.6	1.5	1.49
Proposed inverting (Fig.4)	no	48	71 78	0.3	1.5	1.33
Proposed non-inverting (Fig.5)	no	48	53 49	0.3	1.5	1.33

TABLE III
DCDL PERFORMANCES FOR A 90-nm CMOS TECHNOLOGY (SLOW AND FAST CORNERS)

	slow, 0.9V, 125°C				fast, 1.1V, -40°C			
	t_R (ps)	t_{min} (ps) HL/LH	INL_{max} (ps)	P_D (μW/MHz)	t_R (ps)	t_{min} (ps) HL/LH	INL_{max} (ps)	P_D (μW/MHz)
NAND-based [12]-[15]	82	80 74	1.1	0.77	32	34 32	0.4	1.22
TINV-based [8]	137	44 60	0.6	1.33	48	21 24	0.4	1.99
Proposed inverting (Fig.4)	82	117 126	0.3	1.16	32	48 54	0.3	1.76
Proposed non-inverting (Fig.5)	82	85 79	0.3	1.16	32	37 35	0.3	1.76

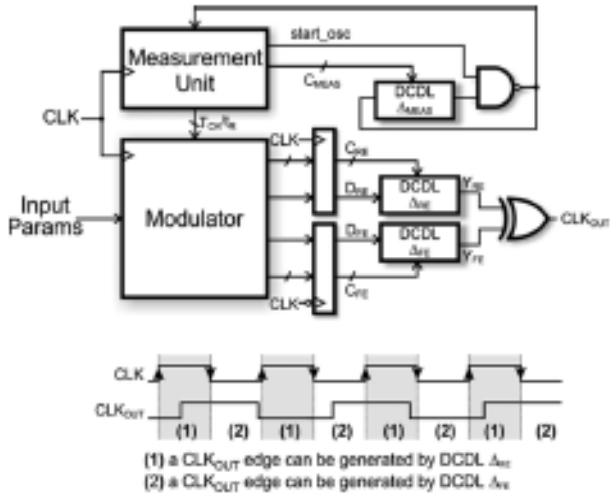

Fig. 6. All-digital SSCG proposed

The Table II compares the performances of proposed DCDLs with previously proposed structures for the typical process corner. From the table it can be noted that, as expected, the proposed solutions achieve the same resolution of NAND-based DCDL, by avoiding its glitching problem. The minimum delay tmin of proposed non-inverting DCDL is very close to tmin of NAND-based DCDL. The lowest tmin is achieved by TINV-based DCDL [8]. This solution, however, pays a 58% higher tr with respect to NAND-based DCDL and a higher power dissipation. Please note that proposed DCDLs result in a lower power dissipation with respect to TINV-based DCDL [8] since transistor sizing can be much more efficient in proposed circuit with respect to TINV-based DCDL, where the PMOS sizing has to be about 2.5 times larger than nMOS. The analysis of the INL data reported in Table II reveals that proposed sizing approach results very effecting, allowing achieving a maximum INL as low as 0.3 ps. The Fig. 11 shows the simulated INL of the proposed non-inverting DCDL. Table III reports the performances of proposed DCDL in slow and fast corners. The most interesting data in this table is the maximum INL, which remains very low, in spite of the large delay variability due to PVT variations. This is a confirmation of the validity of proposed sizing strategy.

V. CONCLUSION & FUTURE WORK

A NAND-based DCDL which avoids the glitching problem of previous circuit has been presented. A timing model of the novel DCDL structure has been developed to demonstrate the glitch-free property of the proposed circuit. As an additional result, the developed model provides also the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation. Three different driving circuits for the DCDL control-bits, which verify the given timing constraints, have been also proposed in the paper. The simulation results confirm the correctness of developed model and show that proposed solutions improve the resolution with respect to previous approaches. As example application proposed DCDL is used to realize an all-digital SSCG. The employ of proposed DCDL in this circuit allowed reducing the peak-to-peak absolute output jitter of more than the 40% with respect to an SSCG using three-state inverter-based DCDLs.

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