International Journal For Technological Research In Engineering
Volume 2, Issue 10, June-2015 *ISSN (Online): 2347 - 4718*

DESIGN OF EFFICIENT SUM OF ABSOLUTE DIFFERENCE ARCHITECTURE FOR H.264/AVC VIDEO CODING

Shruti G Kodiya[1], Dr. Rohini Deshpande[2]
[1]PG Student (M. Tech, VLSI Design & Embedded Systems), [2]Professor & HOD
Department of Electronics and Communication Engineering, East Point College of Engineering and Technology, Bangalore, India

Abstract: This paper presents 4X4 Sum of Absolute Difference (SAD) architecture for motion estimation block of video codec system. . Here the design is optimized for performance as processing time is of priority in high performance video processing applications. The design is explored with two different adder variants. Computation and comparison are performed using Ripple carry adder (RCA) and Carry Select adder (CSLA). Pipelining is also implemented in the design. SAD architecture is modeled using Verilog HDL and verified in the waveform editor of the ModelSim SE 6.3f simulator and synthesized using Xilinx ISE 13.1 by targeting VIRTEX 7 FPGA family. The result analysis shows that SAD architecture with CSLA adder circuit is resulted better performance than RCA.
Keywords: Sum of Absolute Difference (SAD), Ripple carry adder (RCA), Carry Select adder (CSLA)

I. INTRODUCTION

Nowadays multimedia has entered in to many application in the field of medical , electronics industrial, business application such as electronic patient recording (EPR), smart phones, video conferencing, video telephony, digital cameras and so on. The application of multimedia integrate many types of media such as graphics, animation, text, sound, still images and full motion video. In multimedia there is a practical need to store, retrieve and transmit for lage amount of digital data. This need can be accomplished by using the terminology called compression. Video compression is a important compression type in multimedia. The Video compression is used to avoid representing the same or similar video information again and again for example in many cases of video, the video frame will not change much as compared to the adjacent frames. A lot of space will be saved if we can store the similar video information only once. Now matching of similar parts of the video is very important and this can be achieved using motion estimation. Matching process is measured in an objective way using a distortion metric. The Sum of absolute difference (SAD) algorithm is the mostly used distortion metric used in motion estimation. SAD architecture is widely preferable because it consists of only basic arithmetic operations such as addition, subtraction, absolute value etc. These basic arithmetic operations make SAD algorithm fast and suitable for VLSI (very large scale implementation) implementation. There are varieties of video coding standards, the modern video coding standards H.264/AVC is using the Variable block size motion estimation (VBSME). In this new coding standards, there is a significant compression gain compared to older standards, at the cost of a huge computational complexity. In this paper ,4X4 sum of absolute difference is implemented which gives the least sad value and is simulated using modelsim simulation tool and the same is synthesized using xilinx ise tool. The other sections of the paper are organised as follows: section II briefs about the related work. Section III gives the adder exploration. Section IV gives details about sum of absolute difference architecture. Section V describes result and disscussion. Finally paper is concluded in the section VI.

II. RELATED WORK

The work in [1, 2] shows that motion estimation aim at reducing the temporal redundancy between successive frames in video sequence. Innovation has put on improving the video-coding rise to new standard H.264/AVC [3, 4]. In [5] the SAD algorithm has been addressed by implemented it on FPGA. The work in [6] presents a variable block size motion estimation architecture which employs 32-parallel SAD tree with 79% of the total gate count and the power consumption is showed. The work in [7] proposed the SAD architecture using VHDL and utilized for motion estimation block and implemented in FPGA. The author in [8] proposed implementation of the SAD architecture for motion estimation in h.264/avc. Here a high performance and low cost hardware architecture for the real-time implementation of an SAD module based hierarchical ME algorithm for H.264 / MPEG4 Part-10 video coding is implemented.

III. ADDER EXPLORATION

The multi bit binary addition is the most important operation used in arithmetic operation on video codec system. Hence, in most of the video system multi bit adders are critical building block elements. The key challenge addressed in the adder design is the carry propagation involving all operand bits. Various different architecture for multi bit binary addition have been proposed, based upon delay there are two fundamental adder architectures:

A. Ripple carry adder

For an n-bit adder, intermediate carries are generated sequentially. It is simplest architecture. It has longest delay, smallest area and consumes low power. The ripple carry adder architecture is as shown in figure 1.

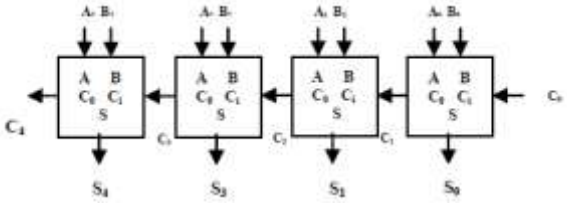

Fig. 1. 4 bit Ripple carry adder architecture

B. Carry select adder

Carry select adder architecture consists of independent generation of sum and carry i.e., C_{in}=1 and C_{in}=0 are executed in parallel. Depending upon the C_{in} the multiplexer select the carry to be propagated to next stage. Further based on the carry input the sum will be selected. Hence the delay is reduced. It consumes more area and power. The carry select adder architecture is as shown in figure 2.

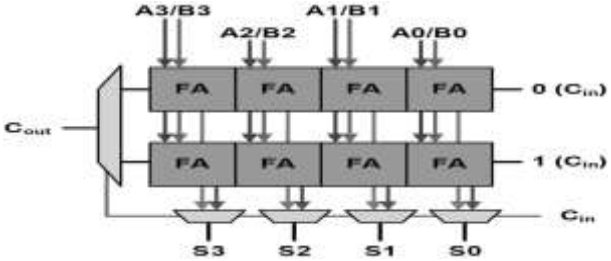

Fig. 2. 4 bit Carry select adder architecture

IV. SUM OF ABSOLUTE DIFFERENCE (SAD) ARCHITECTURE

SAD processor consists of Absolute difference, Sum of absolute differences and Comparator blocks. In SAD processor, the absolute difference block is used to calculate the absolute difference between the reference pixel (template image) block and the corresponding current input pixel (search image) data block in the larger search area. The outputs of each absolute difference unit are added to form the single SAD value. The process is repeated for next input block with reference pixel block. The single SAD values of the each block in the search area are compared using comparator for the minimum SAD value. The corresponding current input pixel data block of the minimum SAD value is considered as the block similar to the reference block against the other SAD blocks. The block size depends on the size of reference block. This paper proposes the 4X4 sum of absolute difference algorithm for motion estimation block of video codec system. The block diagram SAD processor is shown in the figure 3.

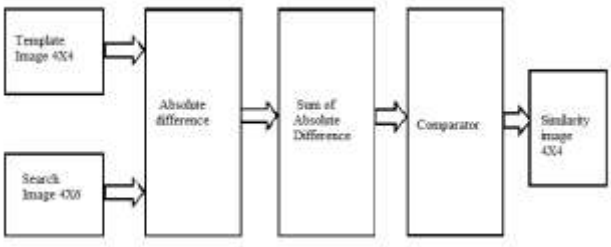

Fig. 3.Block diagram of SAD processor

The SAD processing unit with 16 input samples with 6- stage pipelining is shown in figure 4. The pipelining is the better method to minimize the total time taken for the design and also gives high performance.

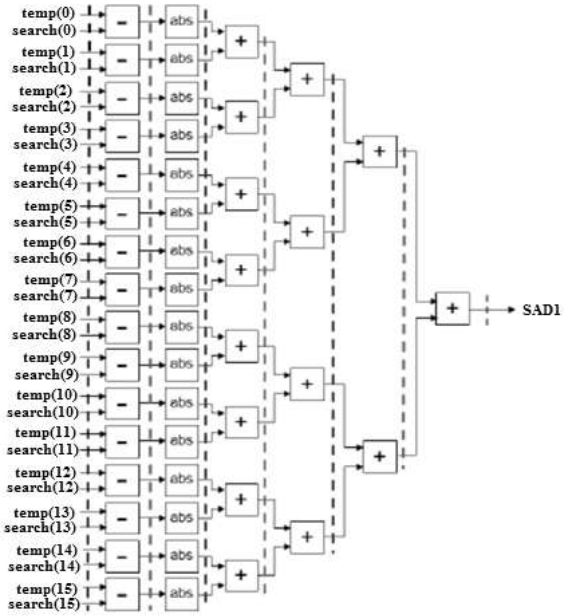

Fig. 4.6- stage Pipelines in a SAD with 16 input samples

V. RESULTS AND DISCUSSION

A. Simulation Results:

1. Simulation Result of 4X4 Sum of absolute difference block with 6- stage pipelining

Figure 5 shows the Simulation result of Sum of absolute difference block with 6-stage pipelining where absolute difference between reference pixel and the current input pixel data block is calculated. Then the output of each absolute difference unit is added to form single SAD value. The output value is displayed after the 6- stage pipelining.

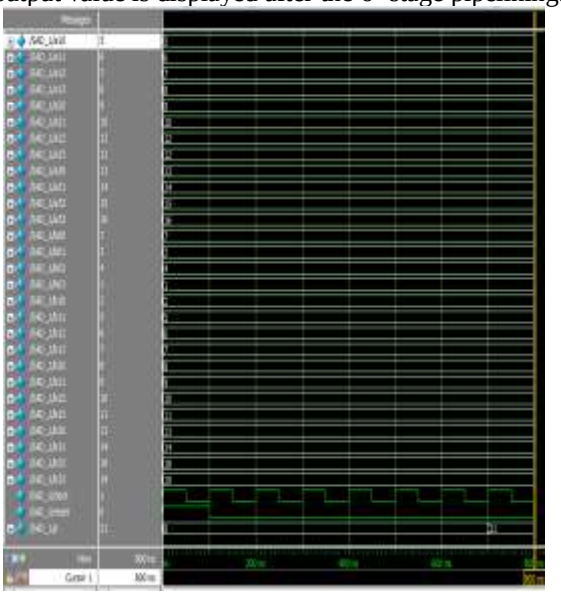

Fig. 5. Simulation result of 4X4 Sum of absolute difference block with 6- stage pipelining

2. Simulation Result of 4X4 Sum of absolute difference Algorithm with 6- stage pipelining

Figure 6 shows the Simulation Result of 4X4 Sum of absolute difference algorithm with 6-stage pipelining where the single SAD values of each 4X4 block in the search area are compared using comparator for the smallest value and similar block values are displayed.

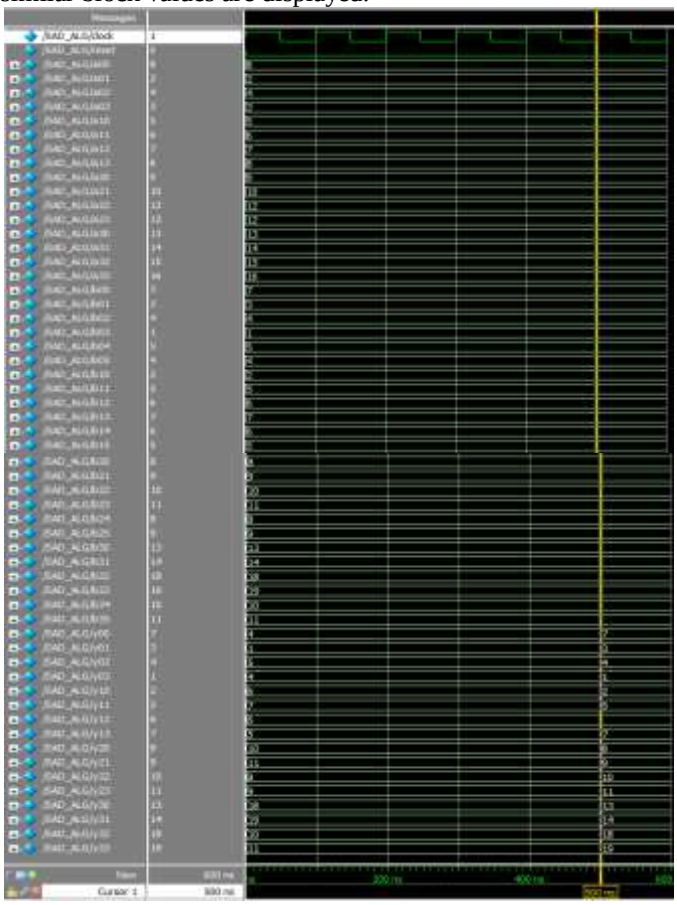

Fig. 6. Simulation Result of 4X4 Sum of absolute difference algorithm with 6- stage pipelining

B. Synthesis results of the SAD with 6-stage pipelining :

Parameters	SAD algorithm with RCA in SAD processor's adder part	SAD algorithm with CSLA in SAD processor's adder part
Area in LUTs	11,019	12,352
Delay in nano seconds	13.754	11.800
Quiescent power in milli watt	558.91	559.29
Dynamic power in milli watt	394.16	405.32
Total power in milli watt	953.07	964.61

VI. CONCLUSION

In this project, 4x4 Sum of absolute difference algorithm for H.264/AVC coding has been implemented. The design is modeled using Verilog HDL and verified in waveform editor of the model-sim 6.3f simulator. Designs were synthesized using Xilinx ISE 13.1 by targeting Virtex 7 FPGA family and results were benchmarked as per the standard FPGA design methodology. Table shows the synthesis results of the SAD architecture with two different adder variants. In the design we have utilized concept of carry select adder to improve the performance of the design and is evident from table that the performance of the design with CSLA is 14.43 % better than the RCA variant.

VII. ACKNOWLEDGEMENT

The authors would like to thank East Point College of Engineering and Technology, Bangalore for their co-operation and support.

REFERENCES

[1] J. Y. Tham et al. "A novel unrestricted center biased diamond search algorithm for block motion estimation," IEEE transactions on circuits and systems for video technology, vol. 8, issue 4, pp 369-377, Aug. 1998.

[2] J. W. Kim et al. "Hierarchical variable block size motion estimation technique for motion sequence coding," optical engineering, vol. 33, pp. 2553-2561, 1994.

[3] H.264 AVC: 'Draft ITU-T recommendation and final draft international standard of joint video specification (ITUT Rec. H.264/ISO/IEC14496-10AVC', in 'Joint Video Team (JVT) of ISO/IECMPE Gland ITU-TVCEG', JVT G050, 2003.

[4] RICHARDSON I.E.G.: 'H.264 and MPEG-4 video compression: video coding for next-generation multimedia' (John Wiley & Sons, 2003).

[5] Stephan Wong, Stamatis Vassiliadis, and Sorin Cotofana "A Sum of Absolute Differences Implementation in FPGA Hardware", International Journal of Electrical and Computer Engineering 4:9 2009.

[6] Z. Liu, et al., "32-Parallel SAD Tree Hardwired Engine for Variable Block Size Motion Estimation in HDTV 1080P Real-Time Encoding Application", IEEE SiPS, 2007, pp. 675-680..

[7] Joaquin Olivares, Ignacio Benavides and et. al. , "Minimum Sum of Absolute Differences implementation in a single FPGA device", Dept. of Electro-technics and Electronics, University of Cordoba, Spain.

[8] R.Mohamed Niyas, M.Guru, P.Jayakrishnan "Implementation of SAD Architecture for Motion Estimation in H.264/AVC", International Journal of Engineering and Technology (IJET) ISSN: 0975-4024,Vol 5 No 2 Apr-May 2013 .

[9] West and Harris, CMOS VLSI Design: a circuits and systems perspective, Addison-Wesley Publishing Company, 3rd ed

