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MODELING OF MULTIPLIER AND ADDER ARCHITECTURE FOR AN EFFICIENT FIR FILTER DESIGN

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Abstract: Most of the Digital signal applications use dedicated processors for the implementation of complex signal processing. Among them, digital filter is also a type, which has the constraint of low power consumption. Since the processing elements are the most copiously used operations in the signal processors, the power consumption of this has the major impact on the system level application. In this paper, we introduce low power concept of Multiplexer based shift/add multiplier to reduce leakage power; and Adder architectures to improve the performance. The proposed concept has lesser leakage power and higher performance of the design. This enabled the design to be dealt with as the low-power corner and can be made adaptable to any level of hierarchical abstractions as per the requirement of the application. The proposed architectures are designed, modeled at RTL level using the Verilog-HDL, synthesized and simulated on Xilinx ISE 13.1 Project navigator tool. Power is analyzed by Xilinx power analyzer. Targeted device is vertex VII xc6vlx75tl.

Keywords: Low Power, Multiplexer based shift/add Multiplier, Carry select Adder, Xilinx ISE power analyzer.

I. INTRODUCTION

The importance of DSP systems with low power, low area and high performance appear to be increasing with no visible sign of saturation. Digital filters play a vital role in digital systems where Finite Impulse Response (FIR) filters are one of the most widely used fundamental devices. The topology of the multiplier circuit also affects the resultant power consumption. Choosing multipliers with more hardware breadth rather than depth would not only reduce the delay, but also the total power consumption. Therefore by reviewing all the above mentioned papers, the low power multiplexer based on shift/add multiplier without clock pulse for reduce dynamic power consumption of a digital FIR filter is a better solution to reduce power. D flip flop is used for delay operation by retaining its stable input registered value. And also pipelining is better topology to minimize the total time taken for the design and also gives high performance. Therefore in our implementation we are using FIR filter design, based on Low Power Multiplexer Base Shift/Add multiplier. And also appropriate adder is chosen which consumes less power and effective performance to increase the speed. Till now, from the adders' survey we found that Carry look ahead and carry select adders are designed for higher performance. Once the implementation of this FIR filter is completed, this filter is compared with other common implementations for area and power.

II. LITERATURE SURVEY

FIR filters are the main computational part of the DSP systems for signal processing. Digital FIR filter design for low power concept has become vast applied technique now days and there are so many proposed research architectures for this low power concept [1], [2], and [4]. There also proposed research architectures for higher performance and low power design [3] and [5]. One of the implementation includes Latch based and pipelining techniques for 6 Tap FIR filter to achieve Low power. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. Digital FIR filter is given with finite state machine input values and filter coefficients. 1-bit MAC unit is designed with enable to reduce the total power consumption. They used MATLAB for filters design and VHDL code for synthesis operation. Active-HDL and Altera Quartus II used for simulation and functional verification is carried out simultaneously. It is seen that Latch based design can reduce the dynamic power consumption [1]. Clock gating and pipelining techniques are used to design and implement FIR filters to achieve low power. MAC unit is the major part of the FIR filter and in the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Multiplier-Accumulator (MAC) unit that consumes low power is always a key to achieve a high performance digital signal processing system. For arithmetic circuits, a large portion of the dynamic power is wasted on un-productive signal glitches. By using pipelining and block reordering methods one can reduce the glitches in the circuits in turn reduce the power consumption. D flip flop is used for clock gating operation [2]. FIR filter is used in many DSP applications and many other synthesis operations of signal require large order FIR filters. The multiplier here they used is Vedic Multiplier. It will reduce the number of partial products generated by a factor of 2. The carry save adder is used in place of adder to avoid the unwanted addition and thus minimize the switching power dissipation. Here they designed FIR filter for 8bit adders and 8bit multiplier and are achieved via VHDL hardware description language using Xilinx ISE software synthesized and implemented on FPGA in Virtex IV family. Also power is analyzed using Xilinx XPower analyzer. The above proposed optimization techniques reduce the power

dissipation in the digital FIR filter[3]. Signal processing in wireless sensor network has a vast range of applications. This [4] reviews several techniques used for designing & implementing low power digital filters for wireless sensor network (WSN). Here they proposed some techniques such as Modified Booth Encoding Algorithm combined with Spurious Power Suppression Technique, Low Power Digit Serial Multiplier along with carry look ahead adder, shift/add multipliers etc. These techniques are used to achieve low power consumption in VLSI-DSP applications, from algorithm and architectural levels to logic, circuits and device levels to reduce power consumption. Another important comparative analysis of Parallel FIR filter [5] deal with the design and implementation of parallel FIR filter structure on FPGA using 4 different parallel processing methodologies with minimal cost of hardware. This deals with the comparative performance analysis of traditional parallel FIR filter with respect to the FFA(Fast FIR Algorithm), transposition and symmetric convolution based parallel FIR filter. By Comparison result they showed that FFA and symmetric convolution based structures save significant number of multipliers with an expense of additional adders and exploits the hardware complexity incurred by the traditional structure.

III. FIR FILTER THEORY

Complex signal processing is the challenging issue in any Digital communication system and there are many individual processors are developed for this processing operation. An information signal is mathematically manipulated by a Digital signal processing (DSP) to modify or improve it in some way. It is characterized by the representation of discrete time, discrete frequency, or other discrete domain signals by a sequence of numbers or symbols and the processing of these signals. The goal of DSP is usually to measure, filter and/or compress continuous real-world analog signals. The enhancement of the input signal is done by a most common processing approach called filtering. So DSP systems are mainly consists of digital filters for signal processing operation. Finite impulse response (FIR) filters are more efficient for signal processing since it is a recursive filter and gives linear phase response and no feedback(poles) reduces the system complexity, stable system always, that are characterized by the extensive sequence of multiplication and addition operations. Due to the strict constraint of devices size and weight we have to concentrate more on power consumption. Hence there is a need for low power consumption devices. Block processing can be applied to digital FIR filters in terms to reduce the power consumption or to increase the performance of the original filter. Based on some applications, FIR filter circuits operates in different sample rates, it may b higher sample rate or low power circuit with moderate sample rate. As we know multiplier and accumulator circuits are effective operators of digital FIR filter, choosing of these device circuits affects the resultant power consumption. We can reduce the delay by choosing multiplier with more hardware breadth rather than depth, also reduce the total power. Digital filtering generally consists of some linear transformation of a number of surrounding samples around the current sample of the input or output signal. The main goal of this work is the high level optimization of filter designs to produce more power efficient results. In Digital filters the modification or alteration of a signal is to be processed in time or frequency domain. The most common digital filter is the linear time-invariant (LTI) filter. An LTI interacts with its input signal through a process called linear convolution, denoted by y=h*x where h is the filter's impulse response, x is the input signal, and y is the convolved output. The linear convolution process is formally defined by:

$y[n] = x[n] \sum_{k=0}^{L-1} h[n] = \sum_{k=0}^{L-1} x[n]h[n-k] = k{=}0L{-}1hkxn{-}k$

…… (1)

An FIR with constant coefficients is an LTI digital filter. The output of an FIR of order or length *L*, to an input time-series $x[n]$, is given by a finite version of the convolution sum given in (1), namely:

$$y[n] = x[n] * h[n] = \sum_{k=0}^{L-1} h[k]x[n-k]$$

…… (2)

where $h[0] \neq 0$ through $h[L-1] \neq 0$ are the filter's L coefficients.

Fig. 1 shows the basic block diagram for an FIR filter of length N. The delays result in operating on prior input samples. The h_k values are the coefficients used for multiplication, so that the output at time n is the summation of all the delayed samples multiplied by the appropriate coefficients.

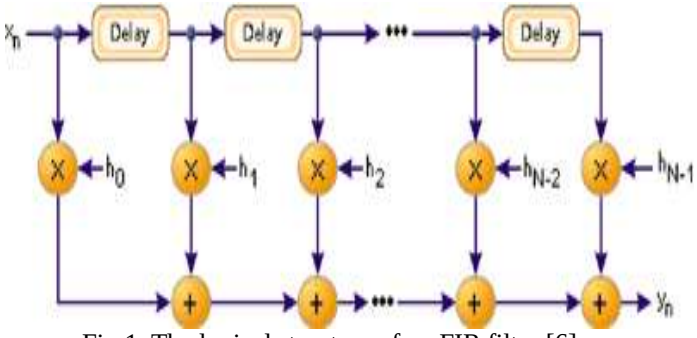

Fig 1. The logical structure of an FIR filter [6]

In this paper, MAC architecture is considered for optimization of multiplier and adder for reduced power and area efficient digital FIR filter architecture.

IV. IMPLEMENTATION DESIGN

There are 3 basic and important building blocks in a FIR filter design are: Multiplication, Addition and a signal delay. And also memory units for storing filter coefficients.

A. Multiplier: Multiplexer based shift/add multiplier

In DSP system there is need for very fast and sufficient precision (bit width; think logic circuits) multiplier to support the particular desired application. In general filter with high quality requires more multiplications. So without multiplier the FIR filter throughput is not completed. Because of its area requirement and higher length for higher

performance operation of multiplier consumes more power in FIR filter. So optimization of this multiplier for low power operation is in high. There are several proposed research architectures developed for this multiplier operation for ex; Array multiplier, Vedic multiplier, Modified booth multiplier, shift/add method and so on. From review of several multiplier architecture multiplexer based shift/add multiplier is much convenient architecture for low power concept. The block diagram of multiplexer based shift/add method is as shown below.

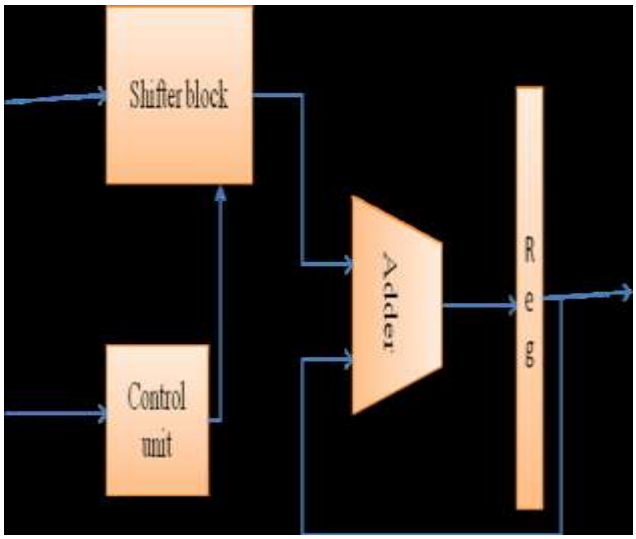

Fig 3 (a): Block diagram of multiplexer base shift/add multiplier for low power [6]

The Multiplier architecture consists of 3 main blocks namely a coefficient, shifter and an adder blocks for the shift/add method. The multiplication with these blocks is elaborated by below example as follows:

Ex: multiply 3x8 for 8 bits of data.

Multiplicand =input=3 and Multiplier =coef=8

Step 1: convert both input and coef into binary form. i.e. input = 00000011 and coef = 00001000

Step 2: consider the coef which is controlled by control unit as shown in figure,

0 0 0 0 1 0 0 0 ⟵ coef

7 6 5 4 3 2 1 0 ⟵ base

Step 3: from looking at base selecting the value of MSB bit of the input coef signal base value. i.e. from this example the coef value of 8 is having MSB bit of 2^3 as its highest base value and the rest coef signals are neglected. Therefore from this the shifting operation of the input given into shifter block is carried out to left side as 3 times.

Step 4: shifting the input signal as 3 times we get the output result

00000011 = 3 ⟵ input signal into shifter block (barrel shifter)

00011000 = 24 ⟵ shifted output value

Shifting operation is done for the input as shown from the example and this is added for the final result.

This shifter block is designed by using multiplexers and the logical diagram of the shifter operation is as shown below:

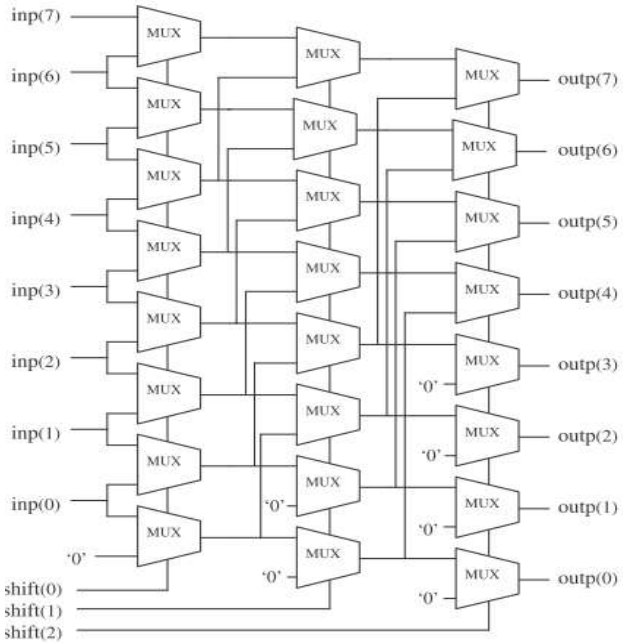

Fig 3 (b): Figure of multiplexer based on shifter block [6]

The shifter design used here is a barrel shifter. It consists of 8 bit input vectors and the output is of 8 bits with shifted version of 8 bits input vector which is controlled by control unit signal base values. For 8 bits data the data shifting is carried out from 0 to 7. This shifter block mainly consists of 3 select lines (individual barrel shifter).one '0' is connected to first MUX (bottom left corner) for the first barrel shifter, second shifter is connected with two '0's to two bottom middle MUX at the bottom and third shifter with four '0's. Similarly for more vector values the shifter block is designed by doubling the number of '0's. For example, shift with '000' has non shift and if shift with '111' cause all barrel shifter to be shifted.

Verilog code implementation for conversion based on power of 2 by control unit:

```
    module shift_mult (p,x,h,clock,reset);
input [7:0] x, h;
input clock, reset;
output reg [15:0] p;
reg [2:0] s;
wire [15:0] q;

always @ (posedge clock)
        begin
            if (reset)
                begin
                    p <= 16'b0;
                end
                else
                begin
                    p <= q;
                end
        end
always @ (h)
        begin
            if (h[7])
```



```
            s[2:0] <= 3'b111;
        else if (h[6])
            s[2:0] <= 3'b110;
        else if (h[5])
            s[2:0] <= 3'b101;
        else if (h[4])
            s[2:0] <= 3'b100;
        else if (h[3])
            s[2:0] <= 3'b011;
        else if (h[2])
            s[2:0] <= 3'b010;
        else if (h[1])
            s[2:0] <= 3'b001;
        else
            s[2:0] <= 3'b000;
    end
bar_shift b_1 (.p(q),.a(x),.s(s) );
endmodule
```

B. Adder architecture

Signal addition is adding of 2 or more signal and is a very basic operation of DSP function. FIR filter consists of an adder as a basic building block and also adders are combined with multiplication operation for adding partial products. Hence MAC (multiply-accumulate) units are features of DSP microprocessors. Generally addition takes place for just 2 inputs operated at a time. Designing of these adders requires more effort because of its critical path. There are several proposed research adder architecture and optimization of this adders are done to increase the design performance of the design. By review of adder architecture, ripple carry adder (RCA) is used for most of the adding operation of processors. Carry look ahead adder (CLA) is another adder which is used for higher order bits for increased performance of the total design. Here we are implementing both RCA and CLA for comparison with better performance. Ripple carry adder is a simpler adder used for adding operation with carry generated by each stage is rippled for next stage. Because of this carry ripple operation foe each stage takes more time makes the RCA slower. But it consumes less power.The block diagram of ripple carry adder is as shown in the figure below:

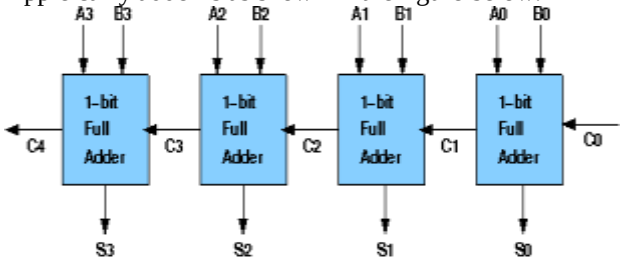

Fig 4 (a): 4-bit Ripple Carry Adder

In digital system a carry-look ahead adder (CLA) is a type of adder used for adding higher bits with increased performance. The wait time required in generating carry bits are overcome from this CLA. This improves speed by comparing with the simpler, but usually slow, ripple carry adder for which the carry bit is calculated side by side with the sum bit, and each bit waits till the previous carry has been calculated. The CLA adder calculates one or more carry bits before doing the actual sum, which minimizes the wait time to calculate the result of the larger value bits. The block diagram of Carry look ahead adder is as shown in the figure below:

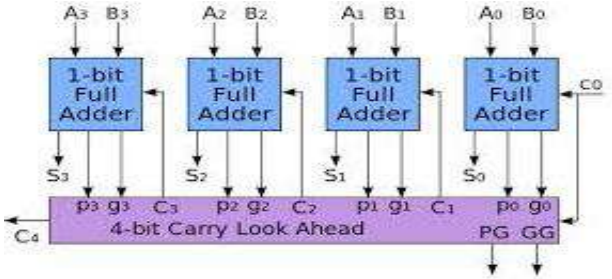

Fig 4 (b): 4-bit Carry Look Ahead Adder [7]

Let ai and bi be the augends and addend inputs, ci the carry input, si and ci+1 , the sum and carry-out to the ith bit location. The pi and gi (auxillary functions) are called the propagate and generate signals, the output of adder is given by:

pi = ai + bi gi = ai bi

si = ai xor bi xor ci ci+1 = gi + pici

C. Signal delay

One sample signal delay is provided by an unit delay. A memory is used for storing sample values per clock cycle and for next cycle this made available as its input signal for processing next stage. N memory cells are required for N unit signal delay. These adder and multiplier designs are implemented into FIR filter and the code is written in verilog-vhdl. The implementation of this FIR filter is carried out by this design flow as shown in the figure below:

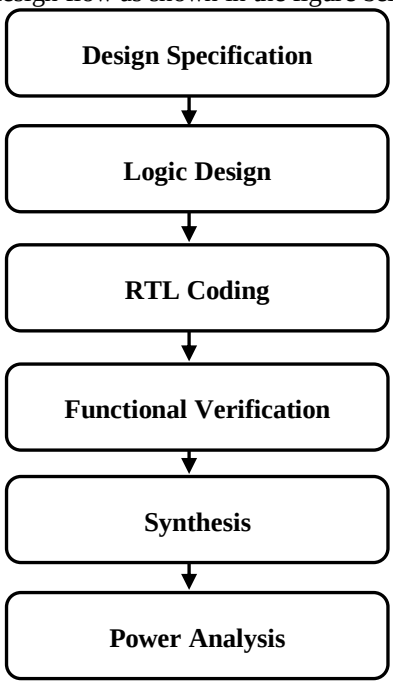

Fig 5: Design & Power Analysis Flow

Modelsim is the tool used for functional verification. Xilinx ISE is the software used for simulation and synthesis operation. Xilinx ISE power analyzer is for power analysis operation and also timing analysis.

V. SYNTHESIS RESULTS AND COMPARISON

Design of an FIR filter is equipped to 8bit input and 8 bit coefficients for 16 taps filter. This accomplished by structural description via Verilog-HDL (hardware description language) by using Xilinx ISE 13.1 software synthesized and targeted on FPGA Virtex VII family. Xilinx XPower analyzer is also used for power analysis. The delay, area and power consumption is obtained from designing of FIR filter with multiplexer based shift/add multiplier and adder (RCA and CLA). The comparison Tables [I, II, III] gives the comparison between power consumption, numbers of LUTs, numbers of Slices for different architectures Table [IV] shows the comparison of our proposed FIR filter architecture results.

TABLE I: SLICES COMPARISONS [7]

Filter(#taps) Virtex IV	Slices (Shift and add)	Slices (MAC)
6	264	219
10	475	418
9	387	462

TABLE II: POWER CONSUMPTION [8]

Digital filter[8]	Power consumption
16-bits coefficient	1248
8-bits coefficient	502
Optimized bit width	450

TABLE III: POWER CONSUMPTION8 TAPS, 16BITS COEFFICION, 8BITS INPUT [9]

Freq	Signed array mult (mw)	Booth without DPDT (mw)	Booth with DRD (mw)	Booth with DPDT using REG (mw)	Booth with DPDT using and gate (mw)
25	612	469	423	326	868
50	1170	879	851	596	669
75	1773	1297	1256	881	1018
100	2293	1703	1658	1137	1283

TABLE IV: CHARACTERISTIC AND POWER CONSUMPTION OF PROPOSED FIR FILTER DESIGN.

FIR FILTER (16TAPS) VIRTEX VII	RCA	CLA
AREA	No. of slice LUT's: 891 No. of slice registers:379	N0. of Slice LUTs:1,038 No. of slice registers:379
DELAY	9.973ns	8.830ns
POWER	Total | Dynamic | Quiescent| --- 574.94 | 28.30 | 546.64	Total | Dynamic |Quiescent | --- 581.72 | 34.86 | 546.86

VI. CONCLUSION

In this paper we are presented an efficient FIR filter for low power and high performance by using a Multiplexer based shift/add multiplier and a sufficient adder for design. The resulted output is compared with other existing parameters. Comparing table [III] and table [IV] for 100 MHz the power is minimized to 545mw. This gives the reduce power consumption of the design. From this comparison table it illustrates that our proposed design approach is very effective with low cost and low power foe implementation of FIR filter. Synthesis operations have been done by Xilinx ISE 13.1 and also power is analyzed by using Xilinx Xpower analyzer. Virtex VII FPGA to target device xc6vlx75tl.

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