

DESIGN HIGH SPEED MULTIPLIER USING VEDIC MATHEMATICS FOR IIR FILTER

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Abstract: Digital signal processing operation utilizing Vedic mathematics which performs the signal handling operation like convolution, circular convolution, cross correlation, auto-correlation and filter design. Digital signal processing (DSP) operations are vital part of engineering and medical field. Outlining of DSP operations have numerous methodologies. This configuration procedure gives the analysis of signals to enhance the accuracy of the mathematical calculations. It encourages the time sharing for all signals to process mathematical operations all the while. Vedic mathematics is the ancient math which has a unique method of mental calculation with the assistance of basic rules and standards based on sutras. The utilization of multiplier has demonstrated the efficiency of Urdhva-Tiryakbhayam method for multiplication which conveys a distinction in the real procedure of multiplication itself. The configuration of IIR filters utilizing Urdhva-Tiryakbhayam sutra. This calculation is performed in Xilinx and compare with MATLAB operation of IIR filter respectively.

Keywords: Vedic Mathematics, Multiplier, DSP, IIR Filter, Urdhva Tiryagbhayam Sutra, MATLAB 8.1, Xilinx 14.5 ISE.

I. INTRODUCTION

Multipliers are basic building blocks of any processor design and normally we called as heart of DSPs. Modern multipliers speed of computation decreases as the inputs increase. There are many multipliers available today like Combinational multiplier, array multiplier, serial and parallel multiplier and many more. Thus building high speed multipliers for processor design is done using Vedic. In DSPs, Filtering is normally used and is applied to many applications like speech processing etc. Digital Signal Processing operations like convolution, Fast Fourier Transform, DFT calculation. Frequency sampling etc method is being used in many applications. Filtering is a method which is used for removing unwanted signal frequencies by being sensitive to the wanted signal frequencies. Digital audio or video when it is transmitted through the communication channel, noisy is added to the original signal. So, at receiver side filtering is must in order to get original one. Basically, filters are Classified into 4 types depending upon the pass band and stopbands. FIR and IIR are two types of filter designed in this paper. Digital signal processing have to perform operations like frequency domain filtering (FIR, IIR) and frequency transformations like DFT, FFT, and DCT. For these operation multiplication is an essential hardware component. Thus the performance of the multiplier is a key element in determining the performance of the entire system. This is

because the multiplier is the slowest and most time consuming element in the system. Thus the optimization of the multiplier speed and area is a major challenge for the system designers. This challenge can be successfully overcome by the use of ancient Vedic mathematics.

II. VEDIC MULTIPLIER

The use of Vedic mathematics is to reduce the typical calculations in conventional mathematics to very simple one. Because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing. A. Urdhva Tiryakbhayam Sutra The proposed Vedic multiplier is based on the "Urdhva Tiryagbhayam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for $n \times n$ bit number. Since the partial products and their sums are calculated in parallel and the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

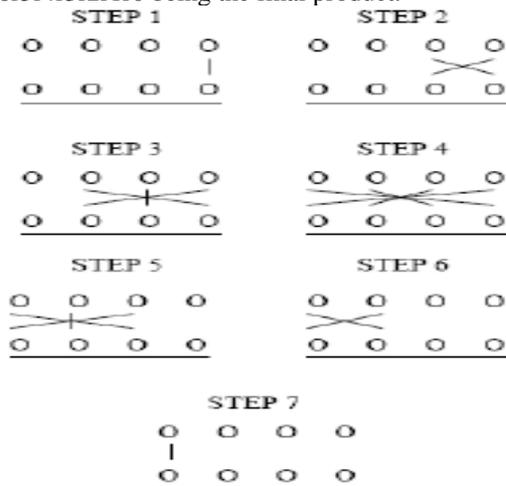
III. URDHVA TIRYAKBHAYAM SUTRA FOR BINARY NUMBER SYSTEM

In this section this Sutra is extended to binary number system. To illustrate the multiplication algorithm, consider the multiplication of two binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$. As the result of this multiplication would be more than 4 bits, let it be as $\dots r_3r_2r_1r_0$. Line diagram for multiplication of two 4-bit numbers is shown in Fig. 2 which is nothing but the mapping of the Fig. 1 in binary system. For

the sake of simplicity, each bit is represented by a circle. Least significant bit r_0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier. The process is followed according to the steps shown in Fig. 2. As in the last case, the digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result (m) and a carry (say c_n). This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and the other entire bits act as carry. For example, if in some intermediate step, we get 110, then 0 will act as result bit and 11 as the carry (referred to as c_n in this text). It should be clearly noted that c_n may be a multi-bit number. Thus the following expressions are coming:

- $r_0 = a_0b_0;$ (1)
- $c_1r_1 = a_1b_0 + a_0b_1;$ (2)
- $c_2r_2 = c_1 + a_2b_0 + a_1b_1 + a_0b_2;$ (3)
- $c_3r_3 = c_2 + a_3b_0 + a_2b_1 + a_1b_2 + a_0b_3;$ (4)
- $c_4r_4 = c_3 + a_3b_1 + a_2b_2 + a_1b_3;$ (5)
- $c_5r_5 = c_4 + a_3b_2 + a_2b_3;$ (6)
- $c_6r_6 = c_5 + a_3b_3$ (7)

With $c_6r_6r_5r_4r_3r_2r_1r_0$ being the final product.

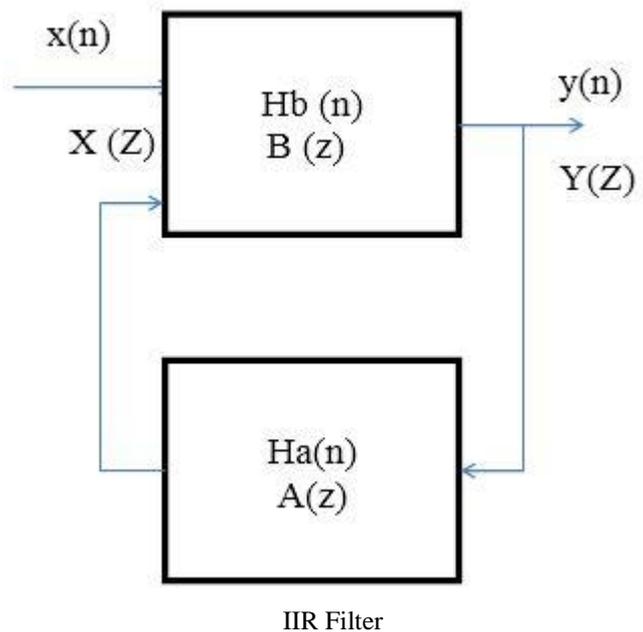


Line diagram for multiplication of two numbers

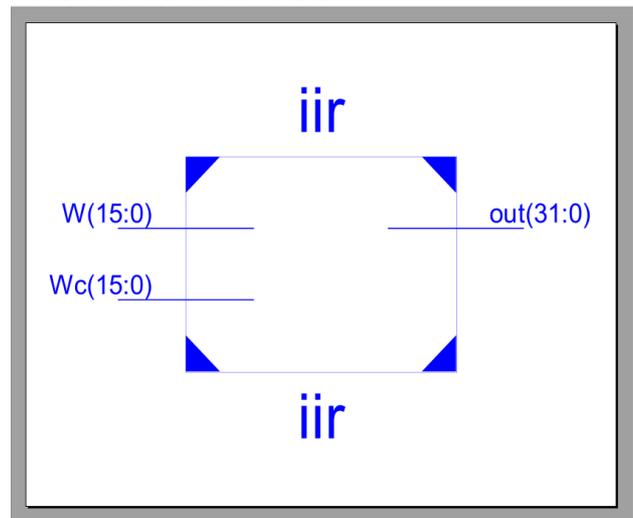
IV. IIR FILTER

IIR filters are digital filters with vast motivation reaction. Dissimilar to FIR filters, they have the feedback and are called recursive digital filters. IIR filters are digital filters with infinite impulse response. Unlike FIR filters, they have the feedback (a recursive part of a filter) and are known as recursive digital filters. Therefore for this reason IIR filters have much better frequency response than FIR filters of the same order. Unlike FIR filters, their phase characteristic is not linear which can cause a problem to the systems which need phase linearity. For this reason, it is not preferable to use IIR filters in digital signal processing when the phase is of the essence. Otherwise, when the linear phase characteristic is not important, the use of IIR filters is an excellent solution. The IIR filters have vastly improved frequency reaction than FIR filters of the same request (order). Dissimilar to FIR filters, their stage trademark (phase

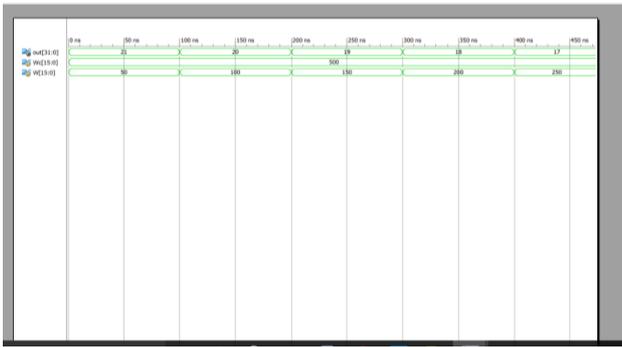
characteristics) is not direct which can bring about an issue to the frameworks which need stage linearity. For this reason, it is not desirable over utilization IIR filters in digital signal when the phase is of the substance. FIR filters can have straight phase trademark that is certainly not of IIR filters. When it is important to have straight phase trademark, FIR filters are the main accessible arrangement. In different situations when straight phase trademark is redundant, for example, FIR filters, speech signal processing is bad arrangement. IIR filters ought to be utilized. The subsequent filter request is significantly lower for the same frequency reaction. The IIR filter transfer function is a proportion of two polynomials of complex variable z^{-1} . The numerator characterizes area of zeros, though the denominator characterizes area of poles of the subsequent IIR filter transfer function.



PERFORMANCE ANALYSIS



Technology Schematic for 16X16 multiplier



Digital Output of 16X16 Multiplier



Analog Output of 16X16 Multiplier

Table 1: 16x16 multiplier using conventional multiplier

| | |
|--------------------------|--------------------------------|
| Number of slices: | 525 out of 704 (74% utilized) |
| Number of 4 input LUT's: | 832 out of 1408 (65% utilized) |
| Number of bonded IOB's: | 105 out of 108 (97% utilized) |

Table 2: 16x16 multiplier using reversible gates

| | |
|--------------------------|-------------------------------|
| Number of slices: | 510 out of 704 (72% utilized) |
| Number of 4 input LUT's: | 893 out of 704 (63% utilized) |
| Number of bonded IOB's: | 65 out of 704 (60% utilized) |

Table 3: Comparison of speed using various multipliers

| Technology used | Maximum Path Delay |
|---------------------------------------|--------------------|
| 2x2 conventional multiplier | 7.167ns |
| 2x2 multiplier using reversible gates | 7.167ns |
| 4x4 conventional multiplier | 13.201 ns |

| | |
|---|-----------|
| 4x4 multiplier using reversible gates | 12.972 ns |
| 8x8 conventional multiplier | 26.177 ns |
| 8x8 multiplier using reversible gates | 24.484 ns |
| 16x16 conventional multiplier | 45.183ns |
| 16x16 multiplier using reversible gates | 40.21ns |

The design and implementation of 16x16 multiplier uses the conventional multiplier which require more hardware (more no. gates), more delay. The table 1 and 2, 3 gives the summary of maximum path delay and no. of slices, LUT's and IOB's for both conventional multiplier and reversible gates which are used in proposed work. Tables shows that the efficiency of reversible gates is more than conventional multiplier as uses less no. of LUTs and IOB's, also makes the speed faster than conventional multiplier.

V. CONCLUSION

The proposed structure of IIR filters utilizing Urdhva Tiryagbhyam sutra of Vedic mathematics. This proposed design is performed in XILINX 14.5 ISE version. The sutras of Vedic mathematics are much more effective than customary mathematics. The Urdhva Tiryagbhyam sutra is faster than the customary method of multiplication. Thus IIR filter based on Vedic sutra taking less average processing time as compared to conventional methods

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