International Journal For Technological Research In Engineering
Volume 5, Issue 9, May-2018 *ISSN (Online): 2347 - 4718*

AN EFFICIENT VLSI IMPLEMENTATION OF BIST BASED ON WEIGHTED PRNG RESEDING

A.D.Durga[1], Dr. K.Gunasekaran[2]
[1]PG Scholar, [2]Professor, M.E., Ph.D, GRT Institute of Engineering and Technology, Tiruttani, India.

ABSTRACT: A new low-power scan-based built-in self test (BIST) technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. During the deterministic BIST phase, the design-for-testability architecture is modified slightly while the linear-feedback shift register is kept short. In both the cases, only a small number of scan chains are activated in a single cycle. Sufficient experimental results are presented to demonstrate the performance of the proposed LP BIST approach. This Proposed design will be implemented by Verilog HDL and simulated by Modelsim Tool. The Proposed Montgomery Multiplier is Synthesis by Xilinx and FPGA Spartan 3 XC 3S 200 TQ 144.
KEYWORDS: BIST , LP Scan , FPGA

I. INTRODUCTION

The gap between functional and test power consumption is growing bigger and bigger, with the latter reaching 2X to 5X of the former due to the ever-shrinking functional power and ever-increasing test power . Problems, such as excessive heat that may reduce circuit reliability, formation of hot spots, difficulty in performance verification, reduction of the product yield and lifetime, and so on, have become severe .. A fast simulation approach was proposed for low-power (LP) off-chip interconnect design. An important through silicon via (TSV) modeling/simulation technique for LP 3- D stacked IC design .Furthermore, the power dissipation of scan-based built-in self-test (BIST) is much higher than power dissipation in deterministic scan testing due to excessive switching activities caused by random patterns. Therefore, it is essential to propose an effective LP BIST approach. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. Weighted pseudorandom testing schemes and methods can effectively improve fault coverage. However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudorandom pattern generator (PRPG).

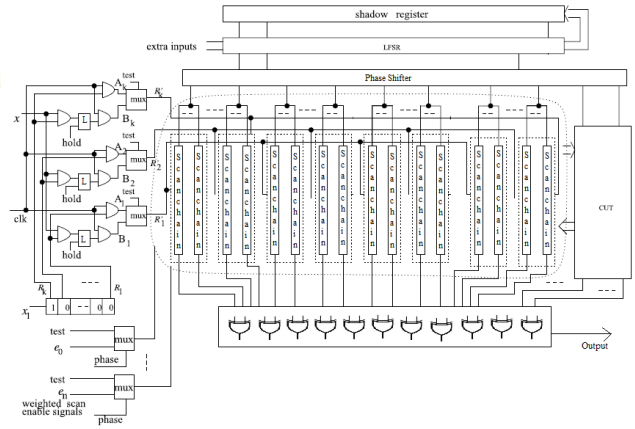
II. RELATED WORKS

Weighted pseudorandom testing schemes can effectively improve fault coverage. A weighted test-enable signal-based pseudorandom test pattern generation scheme was proposed for scan-based BIST, according to which the number of shift cycles and the number of capture cycles in a single test cycle are not fixed. Reconfigurable scan architecture was used for the deterministic BIST scheme using the weighted test enable signal-based pseudorandom test generation scheme. Proposed a new scan segmentation approach for more effective BIST. A novel low-transition linear feedback shift register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak-power reductions with negligible effect on fault coverage or test application time. Experimental results on ISCAS'89 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively.a novel low-transition linear feedback shift register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak-power reductions with negligible effect on fault coverage or test application time. Experimental results on ISCAS'89 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively.

III. PROPOSED METHODOLOGY

A new LP weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using a new clock disabling scheme. The design-for testability (DFT) architecture to implement the LP BIST scheme is presented.

Our method generates a series of degraded sub circuits. The new LP BIST scheme selects weights for the test-enable signals of all scan chains in each of the degraded sub circuits, which are activated to maximize the testability. A new LP deterministic BIST scheme is proposed to encode the deterministic test patterns for random pattern- resistant faults. Only a part of flip flops are activated in each cycle of the whole process of deterministic BIST. A new procedure is proposed to select a primitive polynomial and the number of extra variables injected into the linear-feedback shift register (LFSR) that encode all deterministic patterns. The new LP reseeding scheme can cover a number of vectors with fewer care bits, which allows a small part of flip flops to be activated in any clock cycle.



A new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern Generation and reseeding

MODULES NAME:

- CUT
- MISR
- XOR Network
- LFSR
- Shadow Register & Register
- Scan Chain
- Hold Latch
- Multiplexer

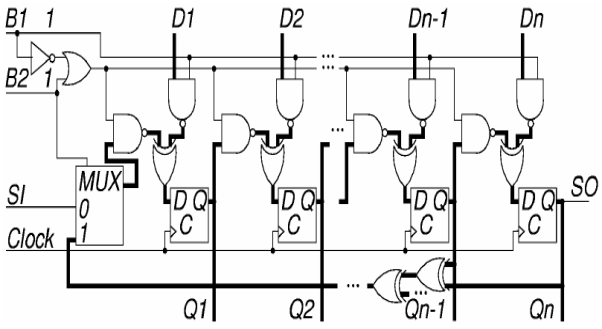
MODULE EXPLANATION:

CUT:

The verification of the circuit under test is done with the test per scan technique. From the scan chains produced from the test per scan method, one of the scan chains is considered as the input to the circuit under test. For testing the circuit, the test patterns generated from the multiple single input change test pattern generator is applied as the input to the CUT. The MSIC sequence generated has the favorable features of uniform distribution and low input transition density. If the produced test patterns of MSIC TPG give the expected output of the circuit under test without any error, a conclusion can be made that the test pattern generation in Built In Self Testing is sound. Reducing the switching activity between the test patterns can reduce the faults in the circuit under test to a great extend by eliminating errors like stuck at faults. MSIC test patterns are single input change vectors that have only single bit transition between test patterns. A combinational circuit is used as the circuit under test. After applying the test patterns from the Multiple Single Input Change to the circuit under test (CUT), the verification of the CUT can be done in two ways. First is by using a reversible technique in the circuit under test. Another method is by using a Look up Table (LUT) method. A typical LUT works as a comparator with stored responses and analyses the test responses to determine the correctness of the CUT.

MULTIPLE INPUT SIGNATURE REGISTER (MISR)

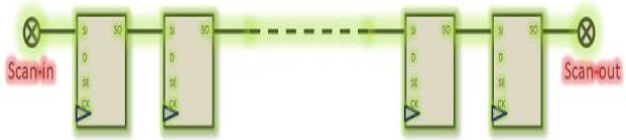
The conventional design of the MISR incorporates a feedback shift register which forms the signature of n-inputs in parallel. The theory of its operation can be stated simply as follows. An n-bit input (one from each input line) is added, modulo 2, to the contents of the n-D-flip-flops (constituting the register). The result is shifted one position before the next word is added. After the last input bit is added, the remaining contents of the D-flip-flops are the aggregated output signature. The initial contents of the flip flops are assumed to be zeros .The modulo 2 adder placed between each of the MISR stages is driven by one of these circuit outputs. The divisor feedback polynomial also feeds the adders at the appropriate stages. This stands against the analysis of the resulting signature. Each input polynomial encounters a different divisor polynomial. Thus, there is little control over the divisor polynomial for each input. Facing different divisor polynomials, one or more of the inputs may encounter a reducible divisor polynomial. Irreducibility is important to catch different types of errors (single bit, double bits, odd number of bits, burst etc.) The test-per-scan scheme, during the testing phase the TPG fills the scan chains which will apply their contents to the circuit under test (CUT). All scan outputs are connected to the multiple input signature register (MISR), which will perform signature compaction. There are possibilities to speed up the test process by using multiple scan chains or by using a partial scan solution. The Design of MISR is shown in Bellow Diagram. For BIST of multiple output circuits, MISR are extensively utilized in practice due to their easy and low cost implementation and efficient fault coverage. MISR, in principle is not different from the single input signature analyzer, but instead of taking one serial input from the first flip-flop, every flip-flop in the MISR has one input coming from the primary outputs of the to be tested circuit as shown in figure



Multiple Input Signature Register

LFSR:
Linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits that appears random and has a very long cycle. Applications of LFSRs include generating pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences. Both hardware and software implementations of LFSRs are common.
SHADDOW REGISTER:
The Shadow Register File Architecture consists of the two register files RF1, RF2 and the Shadow Update Unit (SUU). The SUU is a dedicated hardware unit to update the shadow register file when another process is being executed. The support required from the operating system is that the scheduler should be capable of selecting a group of ready processes for successive execution. The Shadow Register File Architecture has the following characteristics:
• The context switch takes place by switching between the two register files.
• The Shadow Update Unit (SUU) makes ready the register file for the next process to be executed, simultaneously when the current process is being executed.

SCAN CHAINS
Scan chains are the elements in scan-based designs that are used to shift-in and shift-out test data. A scan chain is formed by a number of flops connected back to back in a chain with the output of one flop connected to another. The input of first flop is connected to the input pin of the chip (called scan-in) from where scan data is fed. The output of the last flop is connected to the output pin of the chip (called scan-out) which is used to take the shifted data out. The figure below shows a scan chain.



A scan chain

As said above, scan chains are inserted into designs to shift the test data into the chip and out of the chip. This is done in order to make every point in the chip controllable and observable as discussed below.
SCAN FLOP
The flops in the design have to be modified in order to be put in the scan chains. To do so, the normal input (D) of the flip-flop has to be multiplexed with the scan input. A signal called scan-enable is used to control which input will propagate to the output.

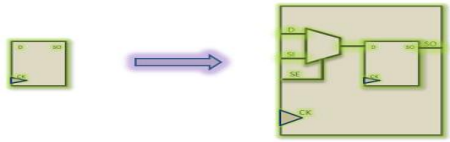


Figure showing transition of a normal flop to scan flop

If scan-enable = 0, data at D pin of the flop will propagate to clock at the next active edge
If scan-enable= 1, data present at scan-in input will propagate to Q at the next active edge
Scan terminology: Before we talk further, it will be useful to know some signals used in scan chains which are as follows:

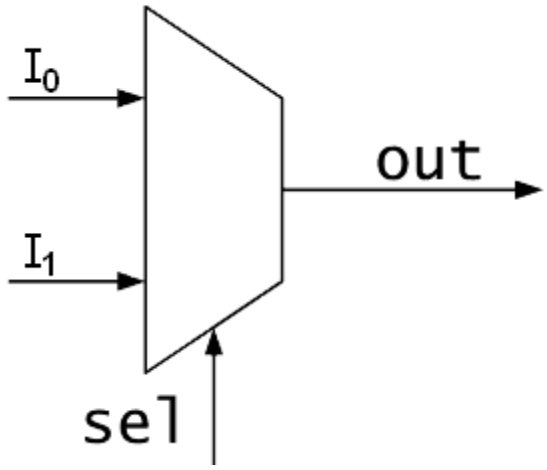
- Scan_in -> Input to the flop/scan-chain that is used to provide scan data into
- Scan_out -> Output from flop/scan-chain that provides the scanned data to the next flop/output
- Scan_enable -> Input to the flop that controls whether scan_in data or functional data will propagate to output

HOLD LATCH:
The D latch (D for "data") or transparent latch is a simple extension of the gated SR latch that removes the possibility of invalid input states. Since the gated SR latch allows us to latch the output without using the S or R inputs, we can remove one of the inputs by driving both the Set and Reset inputs with a complementary driver: we remove one input and automatically make it the inverse of the remaining input. The D latch outputs the D input whenever the Enable line is high, otherwise the output is whatever the D input was when the Enable input was last high. This is why it is also known as a transparent latch - when Enable is asserted, the latch is said to be "transparent" - signals propagate directly through it as if it isn't there.

Enable	D	Q	$\overline{Q}$
0	0	Latched	
0	1	Latched	
1	0	0	1
1	1	1	0

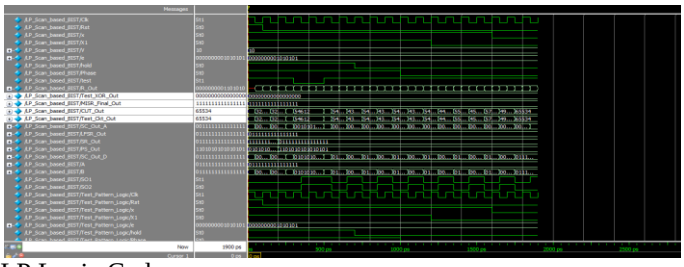
REGISTER:
Registers can be designed using various Flip-Flops (S-R or J-K as D-type) and are also available as MSI devices. Registers in which data are entered or/and taken out in serial form are referred as shift registers, since bits are shifted in the Flip-Flops with the occurrence of clock pulses either in the right direction or in the left direction or in both the directions.

MULTIPLEXERS:
A multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2n inputs has ⌈ n⌉ select lines, which are used to select which input line to send to the output.

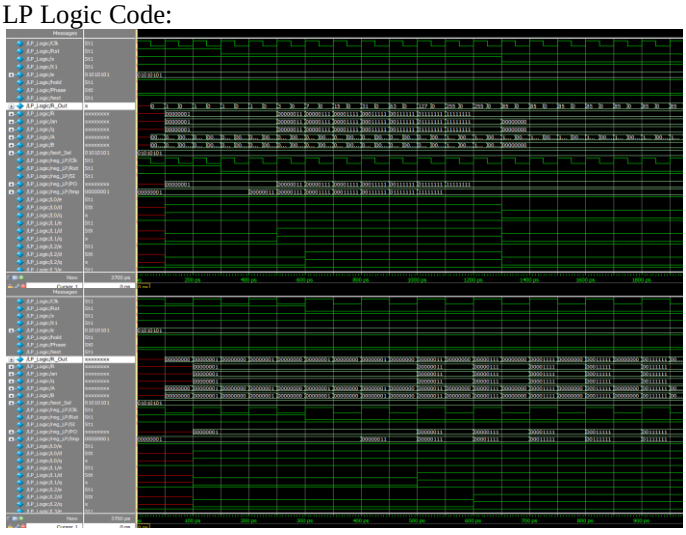


IV. RESULTS AND DISCUSSIONS

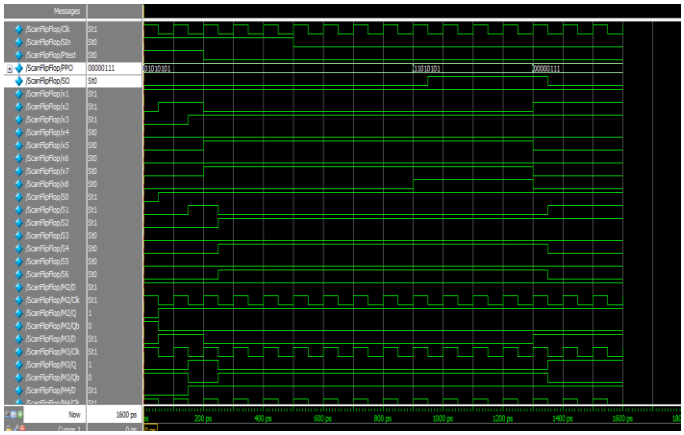
LP Scan based BIST:



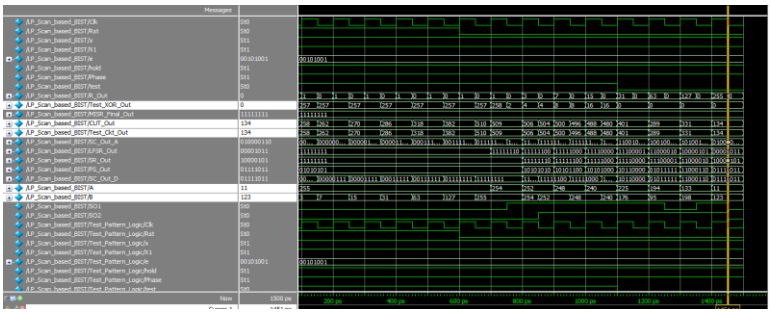
LP Logic Code:



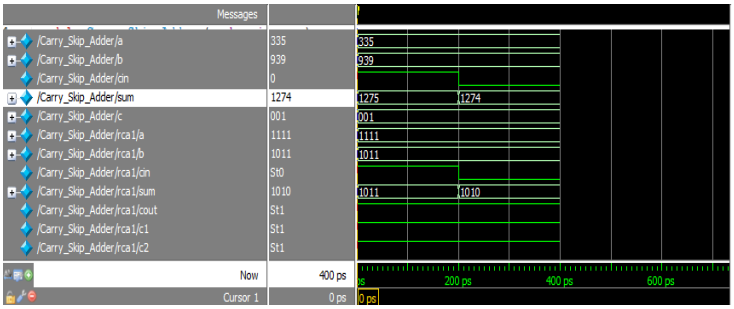
Scan Chain New:



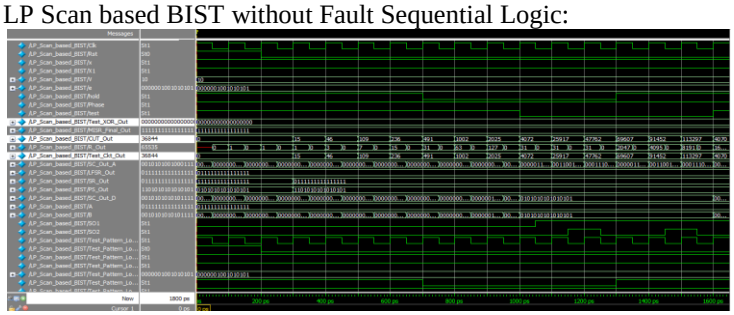
LP Scan based BIST without Fault COMBINATIONAL LOGIC:



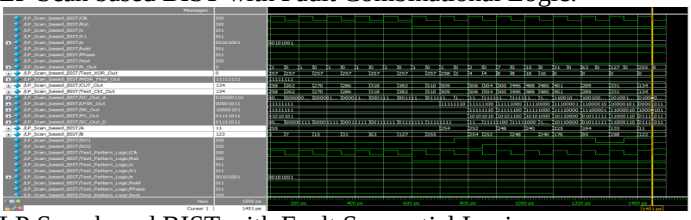
CARRY SKIP ADDER:



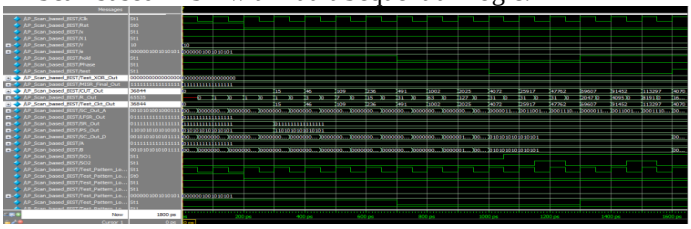
LP Scan based BIST without Fault Sequential Logic:



LP Scan based BIST with Fault Combinational Logic:



LP Scan based BIST with Fault Sequential Logic:



V. CONCLUSION

We proposed a computational technique for EM image segmentation by obtaining dense predictions that combined multi-scale contextual reasoning along with full-resolution reconstruction. Our approach achieved promising performance while relying on minimum post-processing. We expect better probability maps be generated with improvement in the z-dimension resolution of the data provided. A limitation in the underlying post-processing

techniques is that it requires a specific parameter to control the level of over/under segmentation. Automatic tuning of this parameter is not straightforward and can be data-specific even if it is tuned on the validation dataset. We used semi automated visualization of the segmentations to overcome this limitation. Nonetheless, our method can be paired with any other post-processing techniques, leading to an overall performance improvement.

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