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A NOVEL LOW-LEAKAGE AND HIGH-SPEED MULTIPLEXER USING DCVSL LOGIC FAMILY

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Abstract: ***Modern IC design and manufacturing techniques are growing such that the transistor count on a single chip increases exponentially. Ultra-Low Power devices in deep sub-micron technologies used for embedded applications in bio-medical electronics, wireless sensor networks and sophisticated battery operated portable electronic products such as laptops, cell phones, audio-video based multimedia products make power management a critical parameter for test engineers. Sub threshold leakage current increases exponentially in deep-submicron processes and hence is a critical factor in scaling down techniques. Power loss due to leakage is a major problem in deep-submicron technologies as it drains the battery even when a circuit is not operating. Good leakage control mechanisms are necessary to maximize battery life. Modern VLSI ICs are going towards minimizing area, high complexity and high speed circuits as said by Moore. A new differential logic family is devised. The new circuit is simple to design. The circuit topology of the DCVSL and its operation is explained. Its performance in terms of delay and power is compared to that of conventional static logic. Cadence virtuoso simulations using a 45nm technology was utilized to evaluate the performance of the circuits.***

Keywords: ***Differential cascode voltage switch logic(DCVSL), power reduction, sub threshold, leakage power.***

I. INTRODUCTION

Power dissipation has become a very critical design metric with miniaturization. For deep-submicron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. The dynamic (switching) power dissipation is reduced by this to an extent. But the sub threshold leakage current increases exponentially thereby increasing static power dissipation[1]. Leakage current is the current that flows through a transistor when no transactions occur and when the transistor is operating in a steady state. There is exponential variation of Leakage power with threshold voltage and other parameters. The four main components of leakage current in a MOS transistor are [2]:

• Reverse-biased junction leakage current: This occurs from source or drain to the substrate through the reverse-biased diodes when the transistor is off.

• Gate induced drain leakage: This is caused due to the high field effect in the drain junction of MOS transistors. This is increased by high drain to body voltage and high drain to gate voltage.

• Gate direct tunneling leakage: Gate leakage flows from the gate to the substrate through the oxide insulation layer. The PMOS devices have a gate leakage of typically one order of magnitude smaller than that of an NMOS device with identical Tox and Vdd

• Sub threshold (weak inversion) leakage: This is the drain to source current of a transistor operating in the weak inversion region [1].

In this paper, a novel circuit with differential logic is proposed for multiplexer design. The paper is organized as follows. The conventional DCVSL logic cell is described in Section II. In Section III, the design tradeoffs between switching speed and delay in DCVSL cells are discussed. In Section IV, the comparative analysis of novel modified DCVSL multiplexer is done with the conventional multiplexer for various important metrics. The enhancement of signal propagation speed and reduction of leakage power consumption with the modified DCVSL are highlighted. Finally, conclusions are offered in Section V.

II. CONVENTIONAL DCVSL

One of the first realization of static differential CMOS logic known as the Differential Cascode Voltage Switch Logic (DCVSL) was introduced. Since then researchers have shown great interest in differential logic. This is due to its potential to efficiently realize complex logic functions such as XOR/XNOR and multiplexing which form the basic building blocks for most data path units (e.g. adders, multipliers, registers ... etc.). A completion signal is generated when the two rails are different (i.e. after the switching is complete). Also due to their dual rail nature, they can be used to implement self-timed logic. Many changes to the basic DCVSL were proposed to improve its performance. In [3] many of these techniques were evaluated. They ranged from static techniques with reduced internal voltage swings to dynamic techniques with different methods of pre-charging the outputs of the differential gate. However, these techniques add huge design complexity and require complex clocking. In all of these techniques, the dynamic techniques significantly improved the speed but increased the power even further and the static ones slightly improved the speed at the expense of increasing the power consumption. This is due to the increased activity factor (switching probability) resulting from the fact that one of the two outputs of a dynamic differential gate will always switch during evaluation. This property of dynamic circuits has limited its use to highly critical paths where power is

sacrificed for speed.

III. BASIC DCVSL INVERTER

DCVSL circuits have a larger low to high propagation delay than high to low propagation delay and so by increasing the pmos transistor sizing does not necessarily help this problem. The inherent delay problem of DCVSL structures is addressed in [6], [8]. The first paper is proposed to prevent the crowbar current flow (crowbar current is the current from vdd to vss during transition of the gate. There is a time, where both, nmos and pmos is open. This crowbar current gives problem in power dissipation). The second paper is proposed as a solution to prevent the asymmetry between the rising and falling outputs of the circuit. We add a pmos pull-up network to the DCVSL scheme to solve the delay asymmetry problem. However, all of these circuits require a large number of additional transistors, which eliminates the benefit of low transistor count of DCVSL circuits which gives smaller chip area and reduces power dissipation. Higher transistor count also increases internal parasitics, which are a primary concern in RF applications. Fig. 9 shows our proposed solution, DCVSL with resistive enhancement (DCVSL-R), to solve the inherent extra delay component of in DCVSL circuits. The resistors increase the gate overdrive of the pmos load transistors. If we consider the switching conditions of Fig.1 when MN2 turns on and starts conducting current, the gate voltage of MP1 is reduced due to voltage drop at the resistor[9]. For calculating delay in DCVSL circuits, we assumed that the transistors operate in saturation region until the output reaches VDD/2. However, in the DCVSL-R circuit, the drain node of the nmos transistors(also the gate of the pmos transistors)drop quickly and push the transistors into linear region. Now we will explain how the DCVSL-R circuit as shown in fig. 1 improves the propagation delay.By adding the resistors, we put an additional load to the drain of the nmos transistors and increase the voltage drop at the gates of pmos to turn on the pmos transistors faster and minimize this waiting time. Therefore, based on the value of the resistor, we can achieve low to high propagation delay to be equal to high to low propagation delay which results in symmetrical output waveforms. More importantly, due to the reduced low to high propagation delay, the total delay of the DCVSL inverter will be reduced.

Fig.1 DCVSL inverter

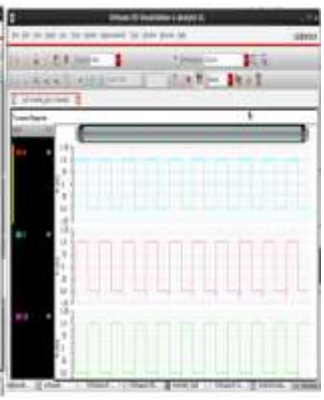

Fig.2 inverter output

IV. MODIFIED DCVSL

MDCVSL stands for modified differential cascode voltage switch logic. If we modify DCVSL circuit by adding two weak p channel devices i.e. transistors T9 and T10 the output of modified DCVSL 2:1 multiplexer will show better results in terms of power consumption, delay, temperature and output load capacitance and operating frequency. The schematic diagram of MDCVSL 2:1multiplexer is shown in Fig.3

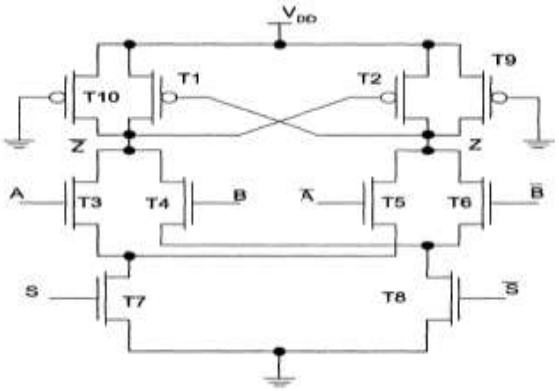

Fig.3 2:1 multiplexer using modified DCVSL

V. COMPARITIVE ANALYSIS

Two multiplexers are designed and compared in this section as shown in fig.4 & fig.5 Above observations will be authenticated with the help of experimental & simulation results drawn by realising multiplexers on cadence VIRTUOSO software with 45nm technology. Schematic Designs & Simulation results are given below for the clear understanding of the multiplexers for the reduction in power requirement.

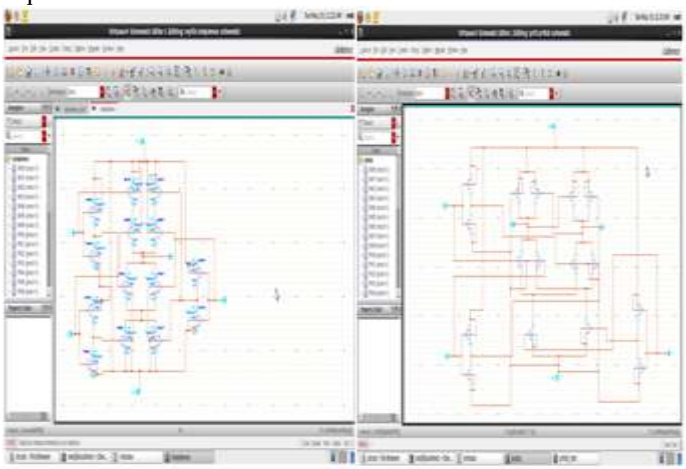

Fig.4 mux using cmos logic
Fig.5 mux using modified DCVSL

Following fact concluded from simulation of multiplexer:

	In CMOS MUX	In modified DCVSL MUX
Power dissipation	17.8E-3	22.06E-6
Delay	23.7E-12	22.5E-12

VI. Table 1. Comparative analysis of multiplexer

VI. CONCLUSION

A modified DCVSL is presented in this paper. By employing this leakage currents are suppressed as compared to the conventional CMOS. DCVSL based inverter has been analyzed and the inherent speed bottleneck of DCVSL structures that cause low to high propagation delay to be greater than high to low propagation delay have been addressed and a solution DCVSL-R that reduces the total propagation delay of the circuit is offered. For low-leakage and high-speed circuits concern should be on both the factors speed and power [12]. This paper concluded with the efficient approach of multiplexer at 45nm technology. Modified Differential Cascade Voltage Switch Logic (MDCVSL) shows least power consumption over a range of power supply voltage, power-delay product over circuit design of 2:1 multiplexer using CMOS logic. Table reveal that the power consumption of the proposed cell is less than that of existing one and thus proves its superiority over existing one and hence ensuring the better performance for low power systems.

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